Exhibit B

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JERRY W. YANCEY ET AL.
Filed:	HEREWITH
For:	RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS
Serial No.:	UNKNOWN
Group Art Unit:	UNKNOWN
Examiner:	UNKNOWN
Atty Docket No.:	LCOM:057

EXPRESS MAIL CERTIFICATION

NUMBER: EV978890499US

I hereby certify that this paper or fee is being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" service, postage prepaid, under 37 C.F.R. 1.10 on the date indicated below and is addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313.

Signature

11/16/06
Date of Deposit

MAIL STOP PATENT APPLICATION
Commissioner For Patents
P. O. Box 1450
Alexandria, VA 22313

Dear Sir:

Transmitted herewith for filing are:

☒ New Continuation-In-Part Patent Application consisting of 54 pages and 18 pages of Figs.

☐ Continued Prosecution Application (37 CFR §1.53(d)) -- The parent application is USSN _____ filed on _____. The prior Examiner was _____ in Group Art Unit _____.

☐ Response to Missing Parts

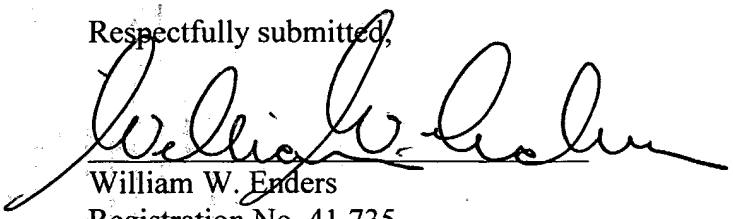
☐ Assignment and Recordation Cover sheet

☐ Inventors' Declaration/Power of Attorney

- ☐ Request and Certification Under 35 U.S.C. 122(b)(2)(B)(i)
- ☒ Information Disclosure Statement, PTO Form 1449; A1-A9; C1-C22
- ☐ Petition for a _____ month extension of time
- ☐ Response to Office Action
- ☐ Preliminary Amendment
- ☐ Formal Drawings
- ☐ Informal Drawings
- ☐ Notice of Appeal
- ☐ An Appeal Brief (an original and two copies)
- ☐ Check in the amount of $
- ☐ The Commissioner is authorized to deduct any requisite fees under 37 CFR 1.16 to 1.21 from, or deposit any credits to, Deposit Account No. 10-1205/ , including any concurrent or future required extension of time fees.
- ☒ In accordance with 37 CFR 1.136(a)(3), the Commissioner is authorized to treat any concurrent or future reply that requires a petition for an extension of time under 37 CFR 1.126(a) to be timely, as incorporating a petition for extension of time for the appropriate length of time, and the Commissioner is authorized to deduct any requisite extension of time fees under 37 CFR 1.16 to 1.21 from Deposit Account No. 10-1205.
- ☒ Postcard. Please date stamp and mail this postcard to acknowledge receipt of the enclosed documents.
- ☐ Other:

The Examiner is invited to contact the undersigned at 512-347-1611 with any questions or comments, or to otherwise facilitate expeditious prosecution of the application.

Respectfully submitted,



William W. Enders
Registration No. 41,735
Attorney for Applicant

O'KEEFE, EGAN & PETERMAN, L.L.P.
1101 Capital of Texas Highway South
Building C, Suite 200
Austin, Texas 78746
512-347-1611
512-347-1615 (Fax)

RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS

by Jerry W. Yancey and Yea Zong Kuo

[0001] This patent application is a continuation-in-part of U.S. Patent Application Serial No. 10/843,226, titled "SYSTEMS AND METHODS FOR NETWORKING MULITPLE FPGA DEVICES," by Jerry W. Yancey, *et al.,* filed on MAY 11, 2004, and which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] This invention relates generally to interconnection of multiple electrical devices, and more particularly to interconnection of multiple ASIC devices, for example, multiple Field Programmable Gate Array (FPGA) devices.

2 Description of the Related Art

[0003] In the past, multiple FPGA devices have been interconnected as an array on a single circuit card using point-to-point or bussed parallel wiring configurations. Such configurations use many wires (along with associated I/O counts and termination components) to achieve required data transfer bandwidths, thus requiring the creation of many connection layers on a circuit card leading to undesirable outcomes such as a high degree of mechanical complexity and cost. Examples of these parallel interfaces include those using signaling standards such as Gunning Transceiver Logic ("GTL"), Stub-Series Termination Logic ("SSTL"), and High-Speed Transceiver Logic ("HSTL"). Some of these standards require as many as three termination components per signal to implement.

[0004] Additional parallel wiring is typically employed when a FPGA array is used to implement multiple card-level interfaces and embedded processor nodes, further increasing circuit complexity. In addition, diverse types of interfaces (VME64x, Race++,

and PCI), processors and user hardware modules are often required to communicate with each other on a single card, further complicating inter-card communications issues. For example, current commercial products commonly bridge two standard interfaces together, such as VERSA-Module Europe ("VME") and Peripheral Component Interconnect ("PCI") interfaces using parallel bridging chips. Additionally, system-level FPGAs with embedded Power PC ("PPC") or similar functions require implementation of more processing and interface nodes on a single card. Banking of I/O pins has reduced the need for termination components, but large I/O counts still require many layers to route, driving printed circuit board ("PCB") layer counts and costs upward.

[0005] In addition to parallel wiring configurations, FPGAs on a single card have been interconnected using IEEE 1149 (Joint Test Action Group -- "JTAG") serial interconnections for configuration purposes. However, such JTAG serial interconnections are not suitable for functions such as high-speed data transfer or signal processing. Thus, the use of multiple large FPGAs, embedded processors, and various standard interfaces on a single card present significant problems with card layout/routing and inter-card communication.

[0006] In large systems, FPGA and other high-performance computing devices are often buried in many layers of custom I/O connections, making them difficult to access for general use. This characteristic comprises many of the benefits realized from using a reconfigurable circuit.

[0007] Medical imaging applications such as Magnetic Resonance Imaging (MRI) and Positron Emission Tomography (PET) are by nature massively parallel calculation-intensive processes. Modern versions of these imaging technologies make extensive use of sophisticated digital signal processing (DSP) algorithms and matrix arithmetic to perform such functions as 3-D reconstruction, color coding, and real-time video display. Seismic oil exploration technology involves not only geology, but also the collection and processing of large amounts of data from geophone and hydrophone

arrays. The analysis and multi-dimensional reconstruction of data from such arrays is a parallel problem which involves sophisticated matrix arithmetic as well as DSP.

[0008] Pharmaceutical and biotech-related applications such as drug interaction modeling and protein folding simulations are at the same time numerous and by nature extremely calculation-intensive. In one example, a simulation which works out the folding sequence for just 50 amino acid molecules (a very limited set compared to the chains which form real proteins) took 4 to 5 days to run. The computational problems with such calculations are so daunting that some researchers have even turned to volunteer computer networks to get more run-time on these simulations. One such group (the "folding@home" project from Stanford), runs protein folding and aggregation simulations by using the internet to access screen saver programs on volunteer PCs which each run a small piece of the overall parallel calculation.

[0009] Special effects in motion pictures and television are also very calculation intensive. Sophisticated effects such as shading, shadowing, texturing, as well as full character animation are becoming increasingly commonplace. One recent movie contained over 6,000 independent artificial intelligence (AI)-driven characters fighting in a lengthy battle sequence. Digital synthesis of a large number of such frames is very costly and time consuming. Because of the long times required to produce the final rendered product, wireframes and other shortcut methods are often used to facilitate the shooting process. As a result, intricate planning and post production is required to make sure that the final effects will fit together with the related live action.

SUMMARY OF THE INVENTION

[0010] Disclosed are methods and systems for interconnecting Application Specific Integrated Circuit ("ASIC") devices using simplex and/or duplex serial I/O connections, including high speed serial connections such as multi-gigabit serial transceiver ("MGT") connections. Examples of ASIC devices that may be interconnected using the disclosed systems and methods include, but are not limited to,

Field Programmable Gate Arrays ("FPGAs") or other field programmable devices ("FPDs") or programmable logic devices ("PLDs"). In one embodiment of the practice of the disclosed systems and methods, serial I/O connections may be employed to interconnect a pair of ASICs to create a low signal count connection. For example, in one exemplary embodiment, high speed serial I/O connections (*e.g.,* such as MGT connections) may be employed to interconnect a pair of ASICs to create a high bandwidth, low signal count connection.

[0011] In one embodiment of the disclosed systems and methods, any given pair of multiple ASIC devices on a single circuit card (*e.g.,* selected from three or more ASIC devices present as a ASIC array on a single circuit card) may be interconnected by one or more serial data communication links (simplex and/or duplex serial data communication links formed between respective serial I/O connections of a given pair of ASIC devices) so that the given pair of ASIC devices may communicate with each other through the two serial I/O connections of each of the serial data communication links with no other serial connection intervening in between, or in other words, in a "one-step" fashion. Such a capability may be implemented, for example, such that each embedded processor, processor node, card level-interface, user-defined hardware module, *etc.* is provided with access to each of the other such entities on the card through one or more separate respective "one step" data communication links that each includes no more than two respective serial connections coupled together (*e.g.,* no more than two respective high speed serial connections coupled together) in the data communication path and through a minimum number of packet transfer points. In a further embodiment, such a respective data communication link may be further characterized as a "direct serial interconnection" between two such entities, meaning that no multi-port switch device (*e.g.,* crossbar switch, *etc.*) exists in the serial data communication path between the boundaries of the two entities. Advantageously, the disclosed systems and methods may be so implemented in one embodiment to achieve communication between given pairs of devices with relatively high data transfer bandwidths and minimal wiring. Furthermore, the disclosed systems and methods may be utilized (*e.g.,* extended) to establish a communications infrastructure across multiple circuit cards.

[0012] The disclosed systems and methods may be implemented in a variety of environments including, but not limited to, signal processing applications, communication applications, interfacing applications, networking applications, cognitive computing applications, test and measurement applications, *etc.* For example, the disclosed systems and methods may be implemented as part of a reconfigurable hardware architecture ("RHA"), such as a reconfigurable signal processing circuit, that serves as a consistent framework in which ASIC applications may be user-defined and/or deployed in such a way as to enhance code portability, design re-use, and intercommunication, as well as to support board-level simulations extending beyond and between individual ASIC boundaries.

[0013] In one embodiment, a RHA may be configured to include a packet-based communications infrastructure that uses a high-bandwidth switch fabric (*e.g.,* crossbar, *etc.*) packet router to establish standard communications protocols between multiple interfaces and/or multiple devices that may be present on a single circuit card (*e.g.,* interfaces, processor nodes, and user-defined functions found on signal processing cards). Such a RHA may be further configured in one embodiment to provide a useful communications framework that promotes commonality across multiple (*e.g.,* all) signal processing applications without restricting user utility. For example, packets conforming to a given interface (*e.g.,* Race++ standard) may be processed by stripping the packet header off and then routing the remaining packet between ASIC devices using the standardized packet router infrastructure of the disclosed methods and systems. Advantageously, such a RHA may be implemented in a manner that does not preclude the addition of high-performance user connectivity, *e.g.,* by only using a relatively small fraction of the available serial I/O connections (*e.g.,* MGT connections) and ASIC (*e.g.,* FPGA) gate resources. In one specific embodiment, embedded serial I/O connections (*e.g.,* embedded MGT connections) of multiple FPGA devices may be used to interconnect the FPGA devices in a manner that advantageously reduces on-card I/O counts and the need for large numbers of termination components. However, it will be

understood that non-embedded serial I/O connections may also be employed in the practice of the disclosed systems and methods.

[0014] In the practice of one exemplary embodiment of the disclosed systems and methods, multiple FPGAs of a FPGA array may be coupled together on a single card to communicate at the card-level basis using packet routing through one or more switch fabrics, *e.g.,* crossbar switches, *etc.* In such an embodiment, each given pair of FPGA devices of a FPGA array may be linked in a manner that advantageously minimizes packet transfer latency times in the switch fabric, while at the same time allowing every source to have access to every destination in the array. In such an embodiment, a universal bridging method may be used in each FPGA to allow intercommunication between any two processors/interfaces on a single circuit card. In one exemplary embodiment, the bridging method may be implemented with a First-In First-Out ("FIFO") packet relay protocol that may be readily integrated into or mapped onto the slave functionality of standard interfaces and/or processor buses.

[0015] Thus, the disclosed systems and methods may be implemented using a predictable and uniform or standardized interface across the boundaries between each pair of board-level components (*e.g.,* FPGAs, ASICs, general-purpose processors, *etc.*) to help promote consistent communications, board-level testability, design portability/re-use, and to provide a user with a relatively high degree of flexibility in establishing functional partitions for hardware modules mapped into an ASIC (*e.g.,* FPGA) array. Further, built-in support for packet integrity checking and automatic retransmission of bad packets may be provided to facilitate the usage of the inter-ASIC links with hardware modules (*e.g.,* signal processors such as Software-Defined Radios(SDRs), signal processing algorithms such as Fast-Fourier Transforms (FFTs) and wavelet transforms, data stream encryption and decryption, packet routing, *etc.*) that are sensitive to data corruption. For example, packet integrity checking (*e.g.,* checksum, CRC, *etc.*) may be incorporated into the hardware layer (*e.g.,* physical layer 1 of Open System Interconnection "OSI" protocol), for example, so that data may be transferred between hardware devices using a packet integrity checking method that is handled automatically

by the hardware without the need for an upper layer of software to perform the packet integrity checking. For example, packet integrity protocol tasks (*e.g.,* such as packet acknowledge, timeout, and retransmit tasks) may be built into interface/interconnection hardware present in a data communication link between ASICs or other devices. Using the configuration of the above-described embodiment, a ASIC array may be configured so as to be easily scaleable to other cards, *e.g.,* permitting expansion of ASIC resources. Where described herein in relation to a FPGA array, it will be understood that the disclosed systems and methods may be implemented with an array of any other type of ASIC device or an array of a combination of types such devices.

[0016] As disclosed herein, reconfigurable communications infrastructures may be implemented to interconnect ASIC devices (*e.g.,* FPGAs) and other computing and input/output devices using high bandwidth interconnection mediums. The disclosed reconfigurable communications infrastructures may be implemented in one embodiment to address communications infrastructure issues associated with interconnecting multiple computing devices such as ASICs. In this regard, the disclosed reconfigurable communications infrastructures may be implemented not only to interconnect ASIC devices that are provided on a single circuit card or that are provided within a single electronics chassis (*e.g.,* provided on separate circuit cards within the same electronics chassis), but also to interconnect ASIC devices and other computing and input/output devices that are positioned in locations that are physically segregated from each other (*e.g.,* that are positioned in different electronics chassis, positioned in different rooms of a given building or facility such as a military base, stationary oil and gas platform, shopping mall, or office building, positioned in different compartments of a given mobile vehicle such as an aircraft, truck and/or trailer, spacecraft, submarine, train, boat, mobile oil and gas platform, *etc.,* and/or that are positioned at different locations using ports across a wide-area network such as the Internet, wireless networks, public telephone system, cable television network, satellite communications system, *etc.*).

[0017] Examples of computing and input/output devices that may be interconnected using the disclosed systems and methods while positioned in locations

that are physically segregated from each other include, but are not limited to, analog/digital converters, digital/analog converters, RF receivers and distribution systems, sensor interfaces and arrays of such devices (*e.g.*, such as antennas, microphones, geophones, hydrophones, magnetic sensors, RFIDs, *etc.*). Other examples of such devices include, but are not limited to, wired network interfaces (*e.g.*, such as Ethernet, Gigabit Ethernet, Universal Serial Bus (USB), Firewire, Infiniband, Serial and Parallel RapidIO, PCIe, Fibre Channel, optical interfaces *etc.*), the Internet, wireless network interfaces (*e.g.*, such as 802.11a, 802.11b, 802.11g, 802.11n, Multiple Input/Multiple Output (MIMO), Ultra-Wideband (UWB), *etc.*), bus interfaces (*e.g.*, such as VME, PCI, ISA, Multibus, *etc.*), compute nodes (including both single and multiple sequential and parallel CPUs), human interface devices (*e.g.*, video displays, manual entry devices, PDAs, cell phones, Personal Computers (PCs), *etc.*).

[0018] For example, in one embodiment of the disclosed systems and methods, a reconfigurable communications infrastructure may be provided to project a reconfigurable network across a wide area. Such a reconfigurable communications infrastructure may be provided, for example, to interconnect physically segregated ASIC devices (*e.g.,* FPGA devices) and other computing devices in a standard and reconfigurable manner. Such an embodiment may be implemented to allow such computing devices to be used in a variety of different arrangements and applications, *e.g.,* for use in any application where a large array of ASIC devices may be usefully employed such as supercomputing, *etc.* To enable interconnection of physically segregated ASIC devices and other computing devices that are physically segregated in relation to each other, high bandwidth interconnection mediums (*e.g.,* such as optical networks and ultra wideband "UWB" wireless networks) may be employed to extend computing device interconnection across relatively large areas and, in one exemplary embodiment to couple together a reconfigurable communications infrastructure with reconfigurable circuits on a large scale.

[0019] In one exemplary embodiment, the disclosed reconfigurable communications infrastructures may be advantageously implemented to enable the

creation of large parallel computing engines in places where they are not currently practical (*e.g.,* such as in aircraft, ship, spacecraft, human-carried and other remote systems). In another exemplary embodiment, ASIC device (*e.g.,* FPGA) "farms" may be created to offer processing services to a wider network. When implemented with a high bandwidth interconnection medium (*e.g.,* an optical interconnect), such interconnected ASIC devices may be physically segregated and widely physically separated to allow ASIC and computing resources of a wide area (*e.g.*, positioned in physically segregated locations within a large vehicle or a building) to be used independently or together, depending on system needs.

[0020] In the practice of the disclosed systems and methods, a reconfigurable network may be implemented using any interconnection medium and/or interface configuration that is suitable for providing high bandwidth communications between computing devices. Examples of suitable high bandwidth interconnection mediums include, but are not limited to, any interconnection mediums (*e.g.,* optical, wired or wireless interconnection mediums) having a data transmission capability of greater than or equal to about 1 gigabit per second (Gbps). Suitable interface configurations that may be employed to implement the disclosed reconfigurable networks include, but are not limited to, a packet router interface switch matrix communications infrastructure as described further herein, or standard interfacing schemes such as Serial Rapid I/O.

[0021] The disclosed systems and methods maybe implemented for a variety of purposes and, in one embodiment, may be employed for distributed, clustered and/or parallel computing tasks. In one embodiment disclosed herein, gate-level reconfigurability may be coupled with a high connection bandwidth and a reconfigurable communications infrastructure to greatly increase the network performance envelope. The reconfigurable nature of the disclosed reconfigurable communications infrastructures may be implemented in one embodiment with a combination of gate-level reconfigurable computing devices (*e.g.,* FPGAs) and high connection bandwidth capability via a high bandwidth interconnection medium to achieve increased performance. In one exemplary implementation, these features may be employed to enable the digital distribution of high

bandwidth data in a manner that minimizes costly RF Distribution systems (RFDs) so that critical signal data is cleaner and more widely accessible.

[0022] In another exemplary implementation, superior performance may be provided in applications where many independent or loosely-coupled processes run in parallel or where a limited amount of hardware is required to perform many different functions. This capability may be employed, for example, in a manner that reduces waste from unused fixed application hardware while increasing processing thread capacity, and/or to allow hardware resources (e.g., computing devices) to be applied in an on-demand fashion, for example, on an as-needed basis to meet varying application requirements and/or to fit the requirements of one or more computing tasks that may exist at any given time. In yet another exemplary implementation, the disclosed reconfigurable communications infrastructures may be utilized to provide a background supercomputing capability, for example, to enable the ability to work certain classes of high-performance signal processing problems that otherwise cannot be worked using conventional computing technology. In this regard, non-active or otherwise-idle "background" processing assets (e.g., processors) may be combined and utilized to construct a background super-processor. Examples of applications in which such a capability may be advantageously implemented include, but are not limited to, applications where processing algorithms are not sample-rate limited, and/or where overhead from parallel processing requirements from working a given problem does not exceed the available calculation overhead. Particular examples of such applications include, but are not limited to, demodulation and analysis of spread-spectrum signals, direct sequence signals, digitally modulated signals, multi-dimensional beamforming, wideband beamforming, large-scale matched filters, low-probability of intercept (LPI) processing, cognitive and artificial intelligence algorithms, back-projection of 3-D images, medical imaging, seismic data processing, protein folding simulations, *etc.*

[0023] The disclosed systems and methods may be implemented in a manner to provide fast external interfaces, large internal interconnection bandwidth, and the ability to perform multiple parallel calculations simultaneously, and thus may be used in one

embodiment to provide an advantageous processing environment for the matrix arithmetic calculations required by medical imaging algorithms, *e.g.,* for parallel calculation-intensive processes such as MRI and PET and to provide 3-D reconstruction, color coding, and real-time video display. Additionally, the dynamic reconfiguration capability offered by the disclosed systems and methods may be used to minimize the size of an imaging processor, making the related equipment more manageable.

[0024] In another embodiment, the disclosed systems and methods may be implemented for collection and parallel processing of large amounts of data from geophone and hydrophone arrays (*e.g.,* using matrix arithmetic) for multi-dimensional reconstruction of this collected data. In this regard, the disclosed systems methods may be so employed to achieve timely processing of collected seismic data in the field to reduce costs over conventional seismic processing methods, to improve collection accuracy, as well as to allow for same-day repositioning of sensors.

[0025] In another embodiment, the disclosed systems and methods may be implemented for computational purposes in pharmaceutical and biotech-related applications, such as drug interaction modeling and protein folding simulations. For example, individual reconfigurable ASIC-based processors may be custom-designed to perform these computation tasks (*e.g.,* so that they each may be employed to run a small piece of an overall parallel pharmaceutical or biotech-related calculation), speeding up the process and making it more cost effective.

[0026] In yet another embodiment, the disclosed systems and methods may be implemented for special effects-related computational purposes, such as shading, shadowing, texturing, and full character animation of AI-driven characters. For such purposes, a large number of frames may be digitally synthesized in a manner more rapid that conventional methods, making "same-day" viewing of the final product possible and in doing so, enhancing creativity by providing a faster turnaround.

[0027] In one respect, disclosed herein is signal processing circuitry including three or more ASIC devices coupled together by one or more serial data communication links so that any given one of the three or more ASIC devices may communicate with any given other one of the three or more ASIC devices through at least one serial data communication link that includes no more than two serial connections.

[0028] In another respect, disclosed herein is a method of processing signals using three or more ASIC devices, the method including communicating signals from each of the three or more ASIC devices to each other one of the three or more ASIC devices through at least one data serial communication link that includes no more than two serial connections.

[0029] In another respect, disclosed herein is an ASIC array, including: three or more ASIC devices, each of the ASIC devices having at least a first serial connection and a second serial connection; wherein a first serial connection of a first one of the three or more ASIC devices is coupled to a first serial connection of a second one of the ASIC devices with no other serial connection therebetween to form a first serial data communication link; wherein a second serial connection of the first one of the three or more ASIC devices is coupled to a first serial connection of a third one of the three or more other ASIC devices with no other serial connection therebetween to form a second serial data communication link; and wherein a second serial connection of the second one of the three or more ASIC devices is coupled to a second serial connection of the third one of the three or more ASIC devices with no other serial connection therebetween to form a third serial data communication link.

[0030] In another respect, disclosed herein is signal processing circuitry including three or more ASIC devices, each one of the three or more ASIC devices including a packet router, the packet router of each one of the three or more ASIC devices being coupled to each respective packet router of the other three or more ASIC devices by a separate respective duplex data communication link so as to form a direct serial interconnection between each two of the three or more ASIC devices.

[0031] In another respect, disclosed herein is a method of routing data packets between three or more ASIC devices of an ASIC array that each include a first serial connection and a second serial connection, the method including: transferring at least one data packet across a first serial data communication link formed between a first serial connection of a first one of the three or more ASIC devices and a first serial connection of a second one of the three or more ASIC devices with no other serial connection therebetween; transferring at least one data packet across a second serial data communication link formed between a second serial connection of the first one of the three or more ASIC devices and a first serial connection of a third one of the three or more other ASIC devices with no other serial connection therebetween; and transferring at least one data packet across a third serial data communication link formed between a second serial connection of the second one of the three or more ASIC devices and a second serial connection of the third one of the three or more ASIC devices with no other serial connection therebetween.

[0032] In another respect, disclosed herein is a method of processing signals using signal processing circuitry including three or more ASIC devices, each one of the three or more ASIC devices including a packet router, and the method including transferring at least one data packet from each the packet router of each one of the three or more ASIC devices to each respective packet router of the other three or more ASIC devices by a separate respective duplex data communication link that forms a direct serial interconnection between each two of the three or more ASIC devices.

[0033] In another respect, disclosed herein is a method, including: providing two or more ASIC devices, each one of the two or more ASIC devices including a packet router; providing a high bandwidth interconnection medium coupled between the packet routers of each of the two or more ASIC devices to form a reconfigurable communications infrastructure; and communicating data between the packet routers of each of the two or more ASIC devices across the high bandwidth interconnection medium.

[0034] In another respect, disclosed herein is a reconfigurable communications infrastructure, including: two or more ASIC devices, each one of the two or more ASIC devices including a packet router; and a high bandwidth interconnection medium coupled between the packet routers of each of the two or more ASIC devices to provide data communication between the packet routers of each of the two or more ASIC devices.

[0035] In another respect, disclosed herein is a communications infrastructure, including two or more ASIC devices, each one of the two or more ASIC devices including a packet router, the packet router of each one of the two or more ASIC devices being coupled to each respective packet router of each of the other of the two or more ASIC devices by an interconnection including a high speed serial optical link.

[0036] In another respect, disclose herein is a method, including: providing two or more ASIC devices, each one of the two or more ASIC devices including a packet router coupled together by an interconnection including a high speed serial optical link, and transferring at least one data packet from each the packet router of each one of the two or more ASIC devices to each respective packet router of each of the other of the two or more ASIC devices by the high speed serial optical link.

BRIEF DESCRIPTION OF THE DRAWINGS

[0037] FIG. 1 illustrates a reconfigurable signal processing circuit according to one exemplary embodiment of the disclosed systems and methods.

[0038] FIG. 2 illustrates a packet router interface switch matrix ("PRISM") communications infrastructure according to one exemplary embodiment of the disclosed systems and methods.

[0039] FIG. 3 illustrates a duplex data communication link according to one exemplary embodiment of the disclosed systems and methods.

[0040] FIG. 4 illustrates a MGT connection core according to one exemplary embodiment of the disclosed systems and methods.

[0041] FIG. 5 illustrates a data packet according to one exemplary embodiment of the disclosed systems and methods.

[0042] FIG. 6 illustrates a data packet header according to one exemplary embodiment of the disclosed systems and methods.

[0043] FIG. 7 illustrates a FPGA device that includes a PRISM router according to one exemplary embodiment of the disclosed systems and methods.

[0044] FIG. 8 illustrates a PRISM router interface wrapper according to one exemplary embodiment of the disclosed systems and methods.

[0045] FIG. 9 illustrates a PRISM router connect multiplexer according to one exemplary embodiment of the disclosed systems and methods.

[0046] FIG. 10 illustrates a PRISM router matrix module according to one exemplary embodiment of the disclosed systems and methods.

[0047] FIG. 11 illustrates a MGT connection module according to one exemplary embodiment of the disclosed systems and methods.

[0048] FIG. 12 illustrates a MGT connection wrapper according to one exemplary embodiment of the disclosed systems and methods.

[0049] FIG. 13 illustrates a reconfigurable communications infrastructure according to one exemplary embodiment of the disclosed systems and methods.

[0050] FIG. 14 illustrates a reconfigurable communications infrastructure according to one exemplary embodiment of the disclosed systems and methods.

[0051] FIG. 15 illustrates a reconfigurable communications infrastructure according to one exemplary embodiment of the disclosed systems and methods.

[0052] FIG. 16 illustrates a reconfigurable communications infrastructure according to one exemplary embodiment of the disclosed systems and methods.

[0053] FIG. 17 illustrates a reconfigurable communications infrastructure according to one exemplary embodiment of the disclosed systems and methods.

[0054] FIG. 18 illustrates a reconfigurable communications infrastructure according to one exemplary embodiment of the disclosed systems and methods.

DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0055] Figure 1 illustrates a reconfigurable signal processing circuit 100 as it may be configured on a single circuit card for reconfigurable signal processing and I/O applications according to one exemplary embodiment of the disclosed systems and methods. As shown in Figure 1, multiple ASIC devices may be provided on a single circuit card, in this exemplary embodiment in the form of four FPGA devices 102, 104, 106 and 108. As will be described further herein, a packet router interface switch matrix ("PRISM") may be provided to route packets between FPGA devices 102, 104, 106 and 108, and other card-level and off-card devices and interfaces in a manner as will be described further herein. As illustrated in the figures herein, arrowhead notation is provided to indicate signal communication with a particular component. In this regard, an arrowhead that intersects a given device or component indicates signal communication to that given component in the direction indicated, while a line without an arrow head indicates that the line passes behind that component, *i.e.,* without signal communication to the component. For example, in Figure 1, duplex serial data communication link 117

is provided between FPGA devices 106 and 108, and duplex serial data communication link 119 is provided between FPGA devices 102 and 108.

[0056] In one exemplary embodiment, each of FPGA devices 102, 104, 106 and 108 may be a Xilinx Virtex-II Pro® XC2VP50 FPGA device (available from Xilinx, Inc. of San Jose, California), and FPGA devices 102, 104, 106 and 108 may be interconnected via high speed serial I/O connections in the form of multiple MGTs that may be interconnected to form data communication links. In this regard, each XC2VP50 FPGA device features a massive programmable logic array, including over 50,000 flip-flops and their associated combinational logic. Additional embedded functions of Xilinx Virtex-II Pro® XC2VP50 FPGA devices include two PowerPC® ("PPC") 405 cores, 232 18X18 multipliers, 4.2 Mb of RAM, 852 user-defined I/O pins, 16 MGTs, and digital clock management.

[0057] When implemented with four Xilinx Virtex-II Pro® XC2VP50 FPGA devices, signal processing circuit 100 of Figure 1 may be configured in one embodiment to accommodate board-level designs in the 15 to 20 million-gate range. However, although the signal processing circuit of Figure 1 is described and illustrated with respect to one particular type of FPGA device, it will be understood that the disclosed systems and methods may be implemented with any other number and/or type/s of multiple ASIC devices that are suitable for card-level interconnection using serial I/O connections. Specific examples of other types of suitable ASIC devices include, but are not limited to, other Virtex-II Pro® devices, Altera Stratix GX® devices, other large FPGAs with high-speed serial I/O, custom ASIC devices with high-speed serial I/O, hardware modules using discrete high-speed serial I/O, *etc.* Further exemplary information on the use of MGT connections on PLD devices as may be employed in the practice of the disclosed systems and methods may be found in United States Patent No. 6,617,877, which is incorporated herein by reference.

[0058] Still referring to Figure 1, each FPGA device 102, 104, 106 and 108 may be configured to have access to respective dedicated memory resources 112, 114, 116 and

118 that may each include, for example, 256 MB of 266 MHz DDR SDRAM and 4 MB of 100 MHz ZBT SRAM. As illustrated, a Compact Flash ("CF") module 120 may be provided for use as non-volatile storage of FPGA configuration data and software. In this regard, a 512 MB CF device may be configured in one exemplary embodiment to store up to 45 configurations for the four-FPGA array of Figure 1, and an automated reconfiguration manager 122 (*e.g.,* Xilinx System Ace®) may be provided to support JTAG communications between the multiple FPGAs and full reconfiguration of the four-FPGA array, *e.g.,* in under 5 seconds. In one exemplary embodiment, the illustrated signal processing circuit embodiment of Figure 1 may be configured to offer a variety of standard interfaces, *e.g.,* including VME64x, PCI, RACE++, parallel Rapid I/O, and high-speed serial standards based on MGTs. In this regard, MGT-based interfaces may include, for example, Fibrechannel, Serial Rapid I/O, XAUI (gigabit Ethernet), Infiniband, and Aurora. The exemplary signal processing circuit 100 of Figure 1 may be provided with at least one PCI Mezzanine Card ("PMC") interface site 124 and/or other type/s of custom interface site/s (not shown) to interface with a wide variety of commercial off-the-shelf ("COTS") devices such as analog/digital converters ("A/Ds"), high-speed I/O, and auxiliary processors/memory (*e.g.,* RAM).

[0059] Also illustrated in the exemplary embodiment of Figure 1 are VME card connector plug jacks (P0, P1, P2), front panel ("FP") connections, RACE interlink 198, and optional parallel I/O paths that may be provided for connection to analyzer probes for test purposes. A custom front panel interface may be provided using any suitable I/O methodology (*e.g.,* MGT serial connection/s, *etc.*). It will be understood that the foregoing components and features are exemplary only, and that any one or more of these components and/or features may be omitted, or that additional components and/or features may be present as so desired or needed to meet the requirements of a given application.

[0060] Figure 2 illustrates one exemplary embodiment of a packet router interface switch matrix ("PRISM") communications infrastructure formed as a part of the RHA of reconfigurable signal processing circuitry 100 of Figure 1, and as it may be implemented

to interconnect multiple FPGAs 102, 104, 106 and 108 of the reconfigurable signal processing circuitry 100 of Figure 1. As further illustrated in Figure 2, in the PRISM infrastructure each FPGA 102, 104, 106 and 108 may be configured with a respective high-bandwidth crossbar router that operates at or near the data transfer bandwidth of the associated high speed interfaces (*e.g.,* about 240 Mbytes / sec or faster). In this regard, each of crossbar routers 202, 204, 206 and 208 may be provided for intra-FPGA communications, and may be provided with MGT connection cores 210 for inter-FPGA communications and communications with other devices.

[0061] As implemented in the exemplary embodiment of Figure 2, the PRISM infrastructure may be configured to interconnect many of (or all) card-level interfaces, processor nodes, and/or user functions related to circuitry 100. In this regard, the PRISM infrastructure may be implemented to provide a useful basic communications framework that promotes commonality across many (or all) applications with little or no restriction to user utility. Further, the PRISM infrastructure may be implemented in a manner that does not preclude the addition of high-performance user connectivity, as it may be implemented to only use a portion of the available MGT and FPGA gate resources.

[0062] Still referring to the exemplary embodiment of Figure 2, a PRISM infrastructure may be implemented in the framework code of each FPGA 102, 104, 106 and 108 in a manner that interconnects many (or all) card-level interfaces, processors, and user-defined functions of signal processing circuitry 100 via MGTs 210 and high-bandwidth packet routers 202, 204, 206 and 208. In this regard, packets may be transferred between PRISM ports in point-to-point fashion, and PRISM hardware may be configured to handle all the details of transmission, including arbitration of packet transfers with the same destination. In this regard, Figure 3 illustrates one exemplary embodiment of a duplex data communication link 300 formed between a given pair of FPGAs 302 and 304 to provide communication between FPGAs 302 and 304 in one embodiment of a PRISM infrastructure matrix. As illustrated, communication between FPGAs 302 and 304 may be accomplished between two full-duplex MGT connection cores 210 (each including respective MGT transmitter 312 and MGT receiver 314) that

form duplex data communication link 300. As illustrated in Figure 3, MGTs 210 may be coupled to logic circuit 330 of respective FPGAs 302 and 304, and may be configured in this embodiment such that communication between FPGAs 302 and 304 is in the form of differential serial signals 318 and 320. It will be understood that two ASIC devices may be interconnected by more than one duplex data communication link (*e.g.,* using two or more pairs of MGT cores 210), and that non-duplex or any other suitable type of communication link/s may be employed in other embodiments to interconnect multiple ASIC devices.

[0063] As shown by the double-arrowhead lines in Figure 2, a packet router interface switch matrix ("PRISM") communications infrastructure may be configured so that one or more direct duplex data communication links exists between any given two ASIC devices, and in this exemplary embodiment between any two FPGAs of multiple FPGAs 102, 104, 106 and 108. For example, duplex data communication link 220 is shown provided between one MGT 210 of PRISM router 202 of FPGA 102 and one MGT 210 of PRISM router 208 of FPGA 108; duplex data communication link 222 is shown provided between one MGT 210 of PRISM router 202 of FPGA 102 and one MGT 210 of PRISM router 206 of FPGA 106; duplex data communication link 224 is shown provided between one MGT 210 of PRISM router 202 of FPGA 102 and one MGT 210 of PRISM router 204 of FPGA 104; duplex data communication link 226 is shown provided between one MGT 210 of PRISM router 204 of FPGA 104 and one MGT 210 of PRISM router 206 of FPGA 106; duplex data communication link 228 is shown provided between one MGT 210 of PRISM router 206 of FPGA 106 and one MGT 210 of PRISM router 208 of FPGA 108; and duplex data communication link 230 is shown provided between one MGT 210 of PRISM router 204 of FPGA 104 and one MGT 210 of PRISM router 208 of FPGA 108. One or more additional duplex data communication links may be optionally provided between respective MGTs 210 of two or more (*e.g.,* between all) of the multiple FPGAs 102, 104, 106 and 108, as shown by the additional dotted and solid double-arrowhead lines in Figure 2.

[0064] As further shown in Figure 2, FPGAs 102, 104, 106 and 108 may be provided with MGTs 210 that form at least one duplex serial link between the User-Defined Functions (152, 154, 156, 158) of each FPGA pair, as well as MGTs 210 that form at least one duplex serial link between the PRISM routers (202, 204, 206, 208) of each FPGA pair, although it will be understood that it is not necessary for a given application that duplex serial links be provided between FPGA User-Defined Functions of given pair/s of FPGAs. Rather, the disclosed systems and methods may be implemented in one alternative embodiment by providing as few as one serial link (*e.g.,* duplex serial link) between pairs of FPGA PRISM routers. It is also possible that one or more data communication link/s (*e.g.,* duplex data communication links) may be provided between FPGA User-Defined Functions of a given pair/s of FPGAs (but not between FPGA PRISM routers), while at the same time one or more duplex data communication link/s may be provided between FPGA PRISM routers (but not FPGA User-Defined Functions) of another given pair/s of FPGAs. Thus, it will be understood that in the practice of the disclosed systems and methods that any FPGA function or embedded module/device on a given FPGA (or other type ASIC) may be linked to any FPGA function or embedded module/device (of the same or different type) on another FPGA (or other ASIC) using one or more serial data communication link/s (*e.g.,* high speed I/O serial data communication links).

[0065] Figure 4 illustrates a serial I/O connection core, in this illustrated exemplary embodiment a MGT connection core 210 (*e.g.,* a Xilinx Virtex-II Pro® MGT connection core), as it may be employed in one exemplary embodiment of the disclosed systems and methods. As illustrated, a MGT connection core 210 may be configured to include transmitter circuitry 312 and receiver circuitry 314. Sixteen such MGT cores 210 are provided in each Xilinx Virtex-II Pro® XC2VP50 FPGA device employed in the illustrated embodiment, although it will be understood that other types of ASIC devices and/or ASIC devices having a different number of serial connections (*e.g.,* MGT connections or other suitable type/s of serial connections) may be employed in the practice of other embodiments of the disclosed systems and methods.

[0066] As shown in the illustrated embodiment of Figure 4, a Xilinx Virtex-II Pro® MGT core 210 may be employed that is configured with respective circuitry 402 and 404 to provide the Physical Coding Sublayer ("PCS") and Physical Media Attachment ("PMA") layers of the Open Systems Interconnection ("OSI") networking model. Such an exemplary MGT connection core 210 may support data transmission rates between 622 Mbps and 3.125 Gbps, and channel bonding between multiple transceivers may also be supported. Multiple clock inputs may be provided to allow for multi-rate operation, *e.g.,* when requirements for low-jitter clocking preclude the use of programmable clocks.

[0067] Still referring to the exemplary Xilinx Virtex-II Pro® MGT core 210 of the embodiment of Figure 4, a MGT transmitter 312 of core 210 may accept input word widths of 8, 16, or 32 bits. When a PRISM infrastructure is configured using such Xilinx MGT cores 210, the infrastructure may be configured in one embodiment so that MGT's 210 use a 32-bit input mode, although any other suitable input mode may be employed in other embodiments. In one exemplary embodiment, commas, clock correction sequences, and packet boundaries may be established via user-defined "K" characters, and a MGT transmitter 312 may include circuitry 406 to replace the last word of the packet with a Cyclical Redundancy Checking ("CRC") word that is used to verify packet integrity in circuitry 408 of MGT receiver 314. An 8B/10B encoder 410 may be used to translate input bytes into 10-bit words prior to serialization, *e.g.,* ensuring no more than 5 consecutive ones or zeros in the resulting serial bit stream. A small FIFO 412 may be provided at the encoder output as an elastic buffer. As shown, MGT transmitter 312 may also be provided with serializer 414 and transmit buffer 416. The final bit stream may be sent as low voltage differential signal ("LVDS") 418, and impedance and pre-emphasis controls may be provided.

[0068] As illustrated, a MGT Receiver 314 may be configured with a receive buffer 422 to accept a LVDS bit stream 420, using an analog phase locked loop ("PLL") to recover the clock and data. A comma detect scheme may be employed to achieve byte alignment on the serial bit stream prior to deserialization in circuitry 424. An 8B/10B

decoder 426 may be used to return the original byte values. Manipulation of pointers in an elastic buffer 428 may be used to support clock correction and channel bonding in circuitry 432. The embedded CRC word in each packet may be checked in circuitry 408 after an end-of-packet K-character ("EOP K-Character") is detected.

[0069] It will be understood with benefit this disclosure that Figure 4 illustrates just one exemplary embodiment of serial I/O connection (*i.e.,* a Xilinx Virtex-II Pro® MGT core) having particular signal handling features as described above that may be employed in a PRISM infrastructure of the disclosed systems and methods. In this regard, it will be understood that any other type of serial I/O connection or serial I/O connection (*e.g.,* having fewer, different and/or additional signal handling features) that is suitable for serial digital signaling may be employed in other embodiments for implementing a PRISM infrastructure. Such serial digital signaling includes, but is not limited to, duplex serial digital signaling at byte transfer rates higher than the associated parallel interfaces. Examples of other suitable serial I/O connections include, but are not limited to, RS-232, AMD TAXI® , Hewlett-Packard G-Link, Fibrechannel FC-0, embedded microprocessor serial interfaces such as Texas Instruments' TMS320C30 serial links, various high-speed serial optical links, *etc.*

[0070] Figure 5 illustrates one exemplary embodiment of data packet 500 that may be employed for communication in a PRISM infrastructure. In such an embodiment, a PRISM router (*e.g.,* 202, 204, 206, 208 of Figure 2) may be configured to transfer data words from a source to a destination in the form of packets. As illustrated in Figure 5, following the start-of-packet K-character ("SOP K-Character") 501 each PRISM packet may contain a user packet 503 that includes a header 502 and a data payload 504 organized into a series of 32-bit words. Also illustrated are CRC word 506 that may be present before the EOP K-Character 508 to verify packet integrity at the receiver in a manner as previously described. In one embodiment, PRISM packets 500 may range in length from 4 to 511 words.

[0071] Figure 6 illustrates one exemplary embodiment of PRISM data packet header 600. As shown, packet header 600 may contain a routing code that allows the sender to determine the packet's destination within a PRISM infrastructure or matrix. In such an embodiment, packet wrappers, control characters, and associated packet retransmit protocols used in the inter-FPGA duplex data communication links 300 may be invisible to the user, and flow control protocols may be used to ensure that only one packet at a time is present in any of the point-to-point links.

[0072] It will be understood with benefit of this disclosure that Figures 5 and 6 illustrate just one exemplary embodiment of the PRISM packet and PRISM packet header that may be employed in the practice of the disclosed systems and methods. In this regard, examples of other suitable data packet configurations that may be employed in a PRISM infrastructure include, but are not limited to, TCP/IP, Fibrechannel, XAUI, Ethernet, Infiniband, Rapid I/O, *etc.*

[0073] Figure 7 illustrates one exemplary embodiment of a PRISM router configuration 702 that may be used to transfer data packets within a PRISM infrastructure to interconnect multiple ASIC devices, *e.g.,* to interconnect multiple FPGAs 102, 104, 106 and 108 of the reconfigurable signal processing circuitry 100 of Figure 1. As shown in Figure 7, each ASIC device (*e.g.,* FPGA 700 of an FPGA array or other configuration of multiple ASIC devices) may be configured to include a PRISM router 702 that interconnects its card-level interface/s 710, processor/s 712, user function/s 714, and inter-FPGA MGTs 704. As shown for the exemplary embodiment of Figure 7, PRISM router 702 may be configured to connect to MGTs 704, card-level interface/s 710, processor/s 712, and/or user-defined function/s 714 via source FIFO interfaces 720 and destination FIFO interfaces 721, and so that all PRISM interface ports share a similar structure as illustrated by PRISM router interface wrapper 800 of Figure 8. In this regard, PRISM router 702 may be configured to see read and write interface ports 830 and 832 (*e.g.,* router interface ports with MGTs 704, card-level interface/s 710, processor/s 712, user-defined function/s 714, *etc.*) as packet sources and destinations. In such an embodiment, interface modules may have source and destination FIFOs 720 and

721 mapped as slave functions, and users may read/write PRISM packets via these slave interfaces.

[0074] The disclosed systems and methods may be implemented using a PRISM communications infrastructure to distribute command/control packets in a manner that supports tasks such as reporting of status and command functions. For example, referring to the exemplary embodiment of Figure 8, a datapath configuration scheme may be implemented via the PRISM matrix using status interface 810 and control interface 812. In this regard, control interface 812 may be provided to intercept control register packets (*e.g.,* command packets provided by a user) that may be used for controlling PRISM matrix operations and/or user defined function operations. Similarly, status interface 810 may be provided to read status register packets transferred via the PRISM matrix. Advantageously, such a datapath configuration scheme may be implemented to achieve simplified operation and circuit layout, *e.g.,* as compared to implementation of control and status tasks using host control register bus, or daisy chain topology.

[0075] In one embodiment of the disclosed systems and methods, a PRISM routing scheme may be configured so that each pair of FPGAs on a given circuit card share a duplex data communication link, and so that no matter what its source is, a packet will cross no more than one duplex data communication link to reach any destination in the PRISM matrix. In this regard, a packet may be routed from a given source to a given destination using any methodology suitable for reading packets from a given PRISM router input or "reader" interface (*e.g.,* from a source FIFO attached to a PRISM router input interface as illustrated in Figure 7), and for writing the packets to a given PRISM router output or "writer" interface (*e.g.,* to a destination FIFO attached to a PRISM router output interface). Thus, in one embodiment, a "reader interface" may be characterized as an interface used to read packets from a FIFO attached to a PRISM router input, and a "writer interface" may be characterized as an interface used to write packets to a FIFO attached to a PRISM router output. However, it will be understood that any other type of packet transmission (*e.g.,* packet queuing and/or arbitration) techniques other than FIFO may be employed that is suitable for reading packets from a PRISM router input and/or

writing packets to a PRISM router output. Examples of such alternative techniques include, but are not limited to, Dual-Port RAM, microprocessor-controlled RAM buffers, register banks, *etc.*

[0076] It will be understood that a PRISM routing scheme may be optionally configured with additional routing capability. For example, when insufficient bandwidth is provided by all available direct duplex data communication links between two devices (*e.g.,* between source and destination FPGA devices), additional bandwidth may be obtained by relaying all or a portion of packets through more than one duplex data communication link (*e.g.,* by relaying packets from a source FPGA to a intermediate second FPGA and then to the destination FPGA through the PRISM router/s of one or more other FPGAs). When implemented, such routing decisions may be made manually by the user or automatically by the PRISM router.

[0077] As illustrated in the exemplary embodiment of Figure 9, each packet destination or writer interface 832 of PRISM router 702 may be configured with a connect multiplexer ("mux_connect") 900 that is capable of accessing each available PRISM reader interface 830a to 830n (*e.g.,* each reader interface available in the local FPGA or other local ASIC device). Within a PRISM router 702 there may be multiple such packet destinations or writer interfaces 832 with a respective connect multiplexer 900 assigned to each corresponding packet destination. Using such an exemplary configuration, a packet transfer request may be asserted at a given reader interface 830 of the PRISM router 702 in combination with packet destination information that corresponds to the connect multiplexer 900 of the desired packet destination or writer interface 832.

[0078] As illustrated for the exemplary embodiment of Figure 6, packet destination information may include, for example, both an FPGA destination code and a "local" destination code within the destination FPGA. In one example, the packet destination information may be written so that either the FPGA destination code matches the code for the current FPGA, or in the event that it does not, so that a specific MGT

destination interface is provided. Thus, if the FPGA destination code does not match the code for the current FPGA, then one of the MGT interfaces will match an available MGT and the packet will be routed off the FPGA to the specified MGT destination. Packets so routed and received at an MGT interface are assumed to be at their destination FPGA and are then routed based on the local destination. However, if the FPGA destination code matches the code for the current FPGA, then the local destination code may be used to determine where the packet goes. It will be understood that such a packet routing scheme may be implemented with other types of ASIC devices besides FPGA devices, and that other types of packet routing schemes are also possible.

[0079] Still referring to the exemplary embodiment of Figure 9, a packet read sequence may begin with a packet source FIFO 720 of a given reader interface 830a asserting a "packet ready" (PR_0) indication 950 to connect multiplexer 900 of a PRISM router 702. At this time, the header word of the packet, presented at DATA input (OUT_BUS_0) 952 of router 702, is assumed to be valid. Assertion of PR_0 indication 950 enables router 702 to transfer the packet as soon as the indicated packet destination (writer interface) 832 is available. The packet is read from the source FIFO 720 one word at a time by asserting the "read enable" control (RD_EN_0) 954. When the entire packet is read from the FIFO 720, the empty indicator (EMPTY_0) 956 is asserted. Assertion of "packet ready clear" (PR_CLR_0) 958 will cause PR_0 950 to be de-asserted to both the source FIFO 720 and to multiplexer 900 of a PRISM router 702. Router 702 will then wait until the next packet is available.

[0080] A packet write sequence may begin with an inactive "packet ready" (PR) indication 960 from a FIFO 721 of the specified packet destination (writer interface) 832. This serves as a signal to multiplexer 900 of a PRISM router 702 that FIFO 721 of the specified packet destination (writer interface) 832 is ready to accept the next packet. When a packet is available for this destination, multiplexer 900 of a PRISM router 702 writes it at DATA output (IN_BUS) 962 of router 702 to FIFO 721 of packet destination 832 one word at a time by asserting the "write enable" control (WR_EN) indicator 964. Once the packet is written into the FIFO 721 of the specified packet destination 832,

assertion of "packet ready set" (PR_SET) 966 will cause PR 960 to be asserted from FIFO 721. PR 960 is de-asserted by FIFO 721 when it is ready to accept the next packet. Empty indicator (EMPTY) 970 may be asserted by FIFO 721 to indicate that the entire packet has been written to another device from the FIFO 721 of packet destination 832.

[0081] As further shown in Figure 9, connect multiplexer 900 may be configured with an optional state machine 910 to process requests for transfer of packets based on a specified priority scheme (*e.g.*, on a "first-come, first-served" basis). In one exemplary implementation using a "first-come, first-served" priority scheme, simultaneous transfer requests may be arbitrated by state machine 910 based on priority assigned by the priority encoder 920 (*e.g.*, the higher the bit significance in the destination field, the higher the priority). State machine 910 may assert "read enable" control (RD_EN) 932 to demultiplexer 930 in order to read the packet from the selected reader interface 830a-830n. Assertion of "packet ready clear" (PR_CLR) 934 by state machine 910 will cause the packet transfer process to terminate. After the priority determination has been made by the priority encoder 920, state machine 910 may be configured to assert a selector control to the demultiplexer 930 and then lock it in place ("FREEZE" 961) in order to select a reader interface 830a-n for packet transfer. Once a transfer path has been selected, a bit in the packet header may be used to "lock" the point-to-point path, preventing any other source from using the destination. It will be understood that the foregoing priority scheme is exemplary only, and that any other priority scheme (or combination of priority schemes) may be employed that is suitable for processing multiple simultaneous requests for transfer of data packets based on one or more inherent and/or assigned criteria.

[0082] Figure 10 illustrates one exemplary embodiment of a PRISM router matrix module (mux_str) 1000 as may be implemented in the practice of the disclosed systems and methods. As shown in Figure 10, an individual multiplexer connect module 900 (*e.g.*, one of modules 900a to 900n) may be provided within matrix module 1000 for each individual PRISM writer interface 832a to 832n. As further illustrated, signals common to each reader interface 830a to 830n (*e.g.*, such as RD_EN and PR_CLR signals) may be

collected from each multiplexer connect module 900a to 900n and combined within matrix module 1000 (*e.g.,* by signal combiners 1010 and 1012) for each PRISM reader interface 830a to 830n (only signal combiners 1010a and 1012a of PRISM reader interface 830a being illustrated in Figure 10). To help assure portability, the same header word bit assignments may always be used for the same functions, regardless of which FPGA the router is instantiated into. In one embodiment, no one given FPGA uses all of the assigned bits at once and there is one pre-defined user, or "hardware" port. Thus, if more than one user port is required or desired for some reason, bits corresponding to an unused function in the given FPGA may be used for this purpose.

[0083] It will be understood that the embodiments illustrated herein are exemplary only, and that other configurations having fewer features, or having one or more alternative and/or additional optional features may be implemented in the practiced of the disclosed systems and methods. Examples of such optional features include, but are not limited to, multiple-destination broadcasts (*e.g.,* implemented by either setting multiple destination bits in a packet header or by sending special command packets to create a "bucket-brigade" pathway within the PRISM matrix), multiple-FPGA relay modes (*e.g.,* implemented by the use of multiple embedded headers and the header relay bit), and/or extension of an FPGA array to include two or more multiple circuit cards (*e.g.,* implemented by the addition of additional MGT destination codes in the header which correspond to off-card MGT interfaces). Furthermore, in one exemplary embodiment, destination bits may be included in the routing field to support a "bypass" mode in the router that serves to facilitate relay of packets around more direct pathways which may be in use or may be non-functional. Furthermore, in another exemplary embodiment, bits may be included in the routing field to support a "debug" mode in the router that serves to facilitate tracing the source of packets. Furthermore, in another exemplary embodiment, bits may be included in the routing field to support a "command" mode in the router that serves to identify packets which carry command, control, and status information.

[0084] Figure 11 illustrates one exemplary embodiment of a serial I/O connection module in the form of a MGT connection module (mgt_connect) 1100 as it may be implemented using a FPGA MGT core 1110 in the practice of the disclosed systems and methods. When desired, MGT connection module 1110 may be provided to handle occasional bit errors that may be seen in high-speed serial links by providing automatic flow control tasks, *e.g.,* such as packet acknowledge, timeout, and retransmit tasks. MGT connection module 1110 may also be configured to monitor a MGT duplex data communication link between two communicating MGTs for problems such as those related to PLL, byte, and word synchronization.

[0085] As illustrated in Figure 11, transmitter side circuitry 1110 of MGT connection module 1100 may provide a destination FIFO 721 coupled to a PRISM router writer interface 832 that provides for input of packet traffic from a PRISM router 702 to the destination FIFO 721. In such an exemplary embodiment, host configuration of module 1100 may be supported via special configuration packets. Other packets may be written to destination FIFO 721 (*e.g.,* a 512 X 32 FIFO) and sent out via MGT transmitter 312 of MGT core 210 as the data payload of an internal packet format. Packet flow control may be maintained via acknowledge/not-acknowledge (ACK/NACK) protocol. As illustrated loop-back path 1160 may be provided so that FIFO 721 may write a packet back to its own input until receipt thereof is acknowledged and the packet is discarded. Thus, in case a packet needs to be retransmitted due to a bit error, a copy may be kept in FIFO 721 until the packet acknowledge is received.

[0086] Still referring to Figure 11, receiver side circuitry 1120 of MGT connection module 1100 may provide a source FIFO 720 coupled to a PRISM router reader interface 830 that provides for output of packet traffic to a PRISM router 702 from source FIFO 720. In such an exemplary configuration, packets may be received by MGT receiver 314 and placed into source FIFO 720 (*e.g.,* a 512 X 32 FIFO) to be accessed from PRISM router reader interface 830. As shown, word alignment multiplexer 1130 may be provided to manage operation (*e.g.,* 32-bit operation) with MGT core 210. Generation of host status, error monitoring, and packet flow control functions may also

be performed in word alignment multiplexer 1130. Also illustrated in Figure 11 are receiver state machine 1180, transmit state machine 1182 and received (RCVD) and send (SEND) acknowledge (ACK) and not-acknowledge (NACK) signals, as well as write (WR), reset (RST), read (RD) and synchronization (SYNC) signals.

[0087] In the practice of the disclosed systems and methods, two or more serial interface modules may be collected or otherwise assembled into one or more connection wrappers in order to consolidate/share common functions and/or tasks. For example, Figure 12 illustrates one exemplary embodiment of a MGT connection wrapper (mgt_connect_str) 1200 that is configured with multiple MGT connection modules, in this case three MGT connection modules 1100a, 1100b and 1100c. It will be understood that MGT connection wrappers may be alternatively configured with two MGT connection modules or with more than three MGT connection modules in other embodiments. In the illustrated embodiment, the three multiple MGT connection modules 1100a – 1100c are collected into common MGT connection wrapper 1200 in a manner so that they may share clock functions (1202, 1203) and reset functions (1204, 1205). In this regard, Figure 12 shows digital clock manager (DCM) 1203 and serial connection (MGT) reset 1205.

[0088] It will be understood that the particular PRISM router configuration described herein in relation to Figures 9 and 10 is exemplary only, and that any other packer router configuration suitable for transferring data packets within a PRISM infrastructure may be employed in the practice of the disclosed systems and methods. For example, a TCP/IP routing scheme may be implemented by configuring PRISM routers 702 as TCP/IP routers, and by assigning respective TCP/IP addresses to each source and destination device (*e.g.*, each ASIC device such as FPGA) within the PRISM infrastructure.

[0089] Figure 13 shows a reconfigurable communications infrastructure 1300 according to one exemplary embodiment of the disclosed systems and methods. In the embodiment of Figure 13, reconfigurable communications infrastructure 1300 includes at

least four separate signal processing circuits (*e.g.,* four separate circuit cards) 1310, 1312, 1314 and 1316 that are interconnected by a high bandwidth interconnection medium 1350 to form a reconfigurable high bandwidth network. As shown in Figure 13, each of signal processing circuits 1310, 1312, 1314 and 1316 includes at least one computing device and is interconnected to high bandwidth interconnection medium 1350 to enable high bandwidth bi-directional communications 1340, 1342, 1344 and 1346. In this exemplary embodiment, signal processing circuit 1310 includes a single ASIC device in the form of a FPGA 1320, signal processing circuit 1312 includes a single processor device (*e.g.*, CPU, microprocessor), signal processing circuit 1314 includes an array of four ASIC devices in the form of four FPGAs 1320, and signal processing circuit 1316 includes an array of two ASIC devices in the form of two FPGAs 1320.

[0090] It will be understood that the illustrated embodiment of Figure 13 is exemplary only, and that a reconfigurable communications infrastructure may be similarly implemented to interconnect two or more signal processing circuits (*e.g.,* two or more signal processing circuits, three or more signal processing circuits, four or more signal processing circuits, five or more signal processing circuits, *etc.*) by a high bandwidth interconnection medium to form a high bandwidth network. Furthermore, each signal processing circuit may include one or more computing devices including, but not limited to, one or more ASIC (*e.g.,* FPGA devices), one or more processor devices (*e.g.,* one or more CPUs or microprocessors), embedded processing devices (*e.g.,* such as Xilinx Virtex-II Pro PowerPCs, Xilinx Microblaze, Xilinx Picoblaze, Altera Nios, Altera ARM, *etc.*), *etc.* A signal processing circuit may also include one or more other types of devices and input/output devices including, but not limited to, analog/digital converters, digital/analog converters, RF receivers and distribution systems, sensor interfaces and arrays of such devices (*e.g.*, such as antennas, microphones, geophones, hydrophones, magnetic sensors, RFIDs, *etc.*), wired network interfaces (*e.g.*, such as Ethernet, Gigabit Ethernet, Universal Serial Bus (USB), Firewire, Infiniband, Serial and Parallel RapidIO, PCIe, Fibre Channel, optical interfaces, *etc.*), the Internet, wireless network interfaces (*e.g.*, such as 802.11a, 802.11b, 802.11g, 802.11n, Multiple Input/Multiple Output (MIMO), Ultra-Wideband (UWB), *etc.*), bus interfaces (*e.g.*, such as VME, PCI, ISA,

Multibus, *etc.*), compute nodes (including both single and multiple sequential and parallel CPUs), human interface devices (*e.g.*, video displays, manual entry devices, personal data assistants (PDAs), cell phones, Personal Computers (PCs), *etc.*), *etc.*

[0091] Although Figure 13 illustrates each of signal processing circuits 1310, 1312, 1314 and 1316 as circuit cards, it will be understood any given signal processing circuit may be provided in any other suitable alternative form (*e.g.* not on a circuit card) for interconnection of a computing device with a high bandwidth interconnection medium, such as high bandwidth interconnection medium 1350.

[0092] In the practice of the disclosed systems and methods, any two or more computing devices that are physically segregated from each other may be interconnected as a part of a reconfigurable communications infrastructure to form a reconfigurable network. For example, Figure 14 illustrates a reconfigurable communications infrastructure 1300 having high bandwidth interconnection medium 1350 interconnecting two signal processing circuits 1314 and 1316 that are physically segregated from each other as illustrated by a physical segregation point 1410 that is positioned therebetween. The physical segregation point 1410 may span any combination of interfaces to a high bandwidth interconnection medium able to extend the reconfigurable network over long distances or over a wide area, *e.g.*, such as an interface to a bundle of multiplexed optical connections, a wireless network, or a specialized wired connection such as a telephone company trunk line. Examples of possible physical segregation points 1410 are the outer boundary of an electronics chassis or other electronics enclosure that contains one of signal processing circuits 1314 or 1316, the boundary between two rooms within a building, the boundary between two compartments of a vehicle, the interface to a wide-area network, *etc.* Although a physical segregation point is shown in Figure 14, it will be understood that the disclosed systems and methods may be utilized to interconnect any two or more computing devices using a reconfigurable communications infrastructure that are not physically separated by a physical segregation point, *e.g.*, such as two or more circuit cards provided within the same electronics chassis or provided adjacent to each other within the same enclosure, room or compartment.

[0093] In the practice of the disclosed systems and methods, any wired or wireless interconnection medium suitable for providing a high bandwidth interconnection between separate computing devices of a reconfigurable communications infrastructure may be employed, *e.g.,* for the high bandwidth interconnection medium 1350 of Figures 13 and 14. In one exemplary embodiment, a high bandwidth interconnection may be an optical transmission medium, *e.g.,* a fiber optic transmission medium that employs wave division multiplexing (WDM) or dense wave division multiplexing (DWDM) technology, fiber optic ribbon transmission medium that employs parallel optical fibers, *etc.* Other examples of optical transmission mediums include, but are not limited to, wireless optical transmission mediums such as free space optics (FSO) laser communications technology. Non-optical high bandwidth interconnection mediums may also be employed including, but not limited to, high bandwidth wired interconnection technologies such as Ethernet, Gigabit Ethernet, Universal Serial Bus (USB), Firewire, Infiniband, Serial and Parallel RapidIO, PCIe, Fibre Channel, *etc.*, and high bandwidth radio frequency (RF) wireless interconnection technologies such as ultra-wideband wireless (UWB) technology, *etc.* In yet another embodiment, any interconnection medium (*e.g.,* optical, wired or wireless interconnection medium) having a data transmission capability of greater than or equal to about 1 Gbps may be employed as a high bandwidth interconnection medium, although it will be understood that wired or wireless interconnection media having a data transmission capability of less than about 1 Gbps may alternatively be employed in other embodiments.

[0094] Suitable interface configurations that may be employed to implement the disclosed reconfigurable communications infrastructure configurations include, but are not limited to, the reconfigurable hardware architecture (RHA) embodiments illustrated and described in relation to Figures 1-12 herein. As described elsewhere herein, such embodiments may be employed to interconnect multiple ASIC devices (*e.g.*, multiple FPGA devices) of a given reconfigurable signal processing circuit (*e.g.,* such as may be implemented on a circuit card), and/or may be employed to interconnect multiple reconfigurable signal processing circuits (*e.g.,* multiple circuit cards). Other examples of

suitable interfacing schemes for interconnection of multiple reconfigurable signal processing circuits (*e.g.,* circuit cards) include, but are not limited to, standard interfacing schemes such as Serial Rapid I/O, Parallel RapidIO, Infiniband, *etc.*

[0095] Figure 15 illustrates one exemplary embodiment of a reconfigurable communications infrastructure 1300 having reconfigurable signal processing circuits 1310, 1314 and 1316 that are interconnected by high bandwidth interconnection medium 1350, which in one exemplary embodiment may be a fiber optic transmission medium configured for transporting WDM or DWDM optical data communication. As shown in Figure 15, reconfigurable signal processing circuit 1314 includes four FPGA devices that may be configured to communicate with each other in a manner as described for FPGA devices 102, 104, 106 and 108 of Figures 1-12 herein, *i.e.,* with duplex serial data communication links 1520 provided between each given two of FPGA devices 102, 104, 106 and 108 (*e.g.,* via high speed serial I/O connections in the form of MGTs), and with each FPGA being provided with a packet router interface switch matrix ("PRISM") to route packets between each of the individual FPGA devices via respective duplex serial data communication links 1520 as shown, as well as for intra-FPGA communications.

[0096] As further shown in Figure 15, reconfigurable signal processing circuit 1314 also includes a high bandwidth interface 1510 coupled to provide high bandwidth bi-directional communication between high bandwidth interconnection medium 1350 and each FPGA device 1320 of reconfigurable signal processing circuit 1314. High bandwidth interface 1510 may be any interface that provides suitable data communication capability between each FPGA device 1320 and high bandwidth interconnection medium 135. For example, in an embodiment where high bandwidth interconnection medium 1350 is an optical data transmission medium, high bandwidth interface 1510 may be an electro-optical interface device such as a device configured according to the XENPAK Multi-Source Agreement (MSA), Fibre Channel, *etc.* In one exemplary embodiment, a reconfigurable signal processing circuit 1310, 1314 and/or 1316 may be configured as illustrated and described in relation to Figure 1, in which case PMC interface site 124 of Figure 1 may be configured as a high bandwidth interface 1510

(*e.g.,* as an optical PMC communication device). However, it will be understood with benefit of this disclosure, that a reconfigurable signal processing circuit 1310, 1314 and/or 1316 may be provided with any other configuration of high bandwidth interface 1510 suitable for interconnecting FPGA devices 1320 with high bandwidth interconnection medium 1350.

[0097] Still referring to Figure 15, each of reconfigurable signal processing circuits 1310 and 1316 are configured in a manner similar to reconfigurable signal processing circuit 1314, with the exception that reconfigurable signal processing circuit 1310 includes only a single FPGA device 1320 and signal processing circuit 1316 includes two FPGA devices 1320. It will be understood that the reconfigurable signal processing circuits of Figures 13-15 are exemplary only and that a reconfigurable signal processing circuit may include any number of FPGA and/or other ASIC devices that may be suitably interconnected using the systems and methods disclosed herein, including but not limited to three ASIC devices, five ASIC devices, six ASIC devices, *etc.* Furthermore, other types of computing and input/output devices may be present on a given signal processing circuit, and interconnected with one or more FPGA or other ASIC devices present on the same signal processing circuit, *e.g.,* such as analog/digital converters, digital/analog converters, RF receivers and distribution systems, sensor interfaces and arrays of such devices (*e.g.*, such as antennas, microphones, geophones, hydrophones, magnetic sensors, RFIDs, *etc.*), wired network interfaces (*e.g.*, such as Ethernet, Gigabit Ethernet, Universal Serial Bus (USB), Firewire, Infiniband, Serial and Parallel RapidIO, PCIe, Fibre Channel, optical interfaces, *etc.*), the Internet, wireless network interfaces (*e.g.*, such as 802.11a, 802.11b, 802.11g, 802.11n, Multiple Input/Multiple Output (MIMO), Ultra-Wideband (UWB), etc.), bus interfaces (*e.g.*, such as VME, PCI, ISA, Multibus, *etc.*), compute nodes (including both single and multiple sequential and parallel CPUs), human interface devices (*e.g.*, video displays, manual entry devices, PDAs, cell phones, Personal Computers (PCs), *etc.*), *etc.*

[0098] Each of FPGA devices 1320 of Figures 13-15 may be configured, for example, as shown and described for FPGA 700 Figure 7, *i.e.,* to include a PRISM router

702 that interconnects card-level interface/s 710, processor/s 712, user function/s 714, and inter-FPGA MGTs 704, and that may be configured to connect to MGTs 704, card-level interface/s 710, processor/s 712, and/or user-defined function/s 714 via source FIFO interfaces 720 and destination FIFO interfaces 721. In such a configuration, the PRISM infrastructure (*i.e.,* that includes PRISM routers within each of FPGAs 1320) may be used to transfer data packets in a manner to interconnect an FPGA device 1320 of one of signal processing circuits 1310, 1314 and/or 1316 with an FPGA device 1320 of a different one of signal processing circuits 1310, 1314 and/or 1316 across high bandwidth interconnection medium 1350 of reconfigurable communications infrastructure 1300. The PRISM infrastructure may also be utilized to transfer data packets for intra-FPGA communications as described elsewhere herein. It will be understood that this configuration and methodology described below may be employed to interconnect other types of ASIC or other computing devices of separate signal processing circuits and/or combinations of FPGA devices with other types of ASIC or other computing devices.

[0099] Reconfigurable communications infrastructure 1300 of Figures 13-15 may be configured in one exemplary embodiment with a PRISM routing scheme that provides a duplex data communication link between each FPGA of a given signal processing circuit (*e.g.,* circuit card) and high bandwidth interface 1510 (*e.g.,* PMC interface site 124 of Figure 1) with high bandwidth interconnection medium 1350. In such a configuration, a data packet may be routed from a given source of a source computing device (*e.g.,* FPGA 1320) of a first reconfigurable signal processing circuit to a given destination of a destination computing device (*e.g.,* a different FPGA 1320) of a second reconfigurable signal processing circuit using, for example, PRISM router and data packet configurations illustrated and described herein in relation to Figures 5, 6 and 7. However, it will be understood that any other data packet configuration and routing scheme suitable for allowing a sender or source to determine the packet's destination within a reconfigurable communications infrastructure 1300 may be employed (*e.g.,* TCP/IP, Fibrechannel, XAUI, Ethernet, Infiniband, Rapid I/O, *etc.*). Further information on exemplary methodology and systems that may be employed for relaying data packets in the disclosed systems and methods may be found in United States Patent Application

Serial No. _____, entitled "METHODS AND SYSTEMS FOR RELAYING DATA PACKETS" by Yancey, et al. (Atty. Docket LCOM-056) filed on the same date as the present application and which is incorporated herein by reference.

[00100] In one exemplary embodiment, the disclosed reconfigurable communications infrastructure may be implemented to provide increased inter-device connection bandwidth for board-level, box-level (*i.e.,* chassis-level) and system-level configurations, *e.g.,* by increasing allowable circuit board-to-circuit board physical separation, box-to-box physical separation and/or system-to-system physical separation. For example, communication bandwidths of at least about 200 megabits per second (*e.g.,* alternatively from about 200 megabits per second to about 100 gigabits per second) may be achieved between individual computing devices (*e.g.,* ASIC devices such as FPGA devices) physically separated by a distance of up to about 10 centimeters and alternatively physically separated by a distance of from about 5 centimeters to about 10 centimeters (*e.g.,* computing devices positioned on the same circuit board); communication bandwidths of at least about 50 megabits per second (*e.g.,* alternatively from about 50 megabits per second to about 100 gigabits per second) may be achieved between individual computing devices physically separated by a distance of up to about 1 meter and alternatively physically separated by a distance of from about 10 centimeters to about 1 meter (*e.g.,* computing devices positioned on different circuit boards within a common box or chassis); and communication bandwidths of at least about 12 megabits per second (*e.g.,* alternatively from about 12 megabits per second to about 100 gigabits per second) may be achieved between individual computing devices physically separated by a distance of up to about 100 meters and alternatively physically separated by a distance of from about 1 meter to about 100 meters (*e.g.,* computing devices positioned in different compartments of a given vehicle or positioned in different rooms of given building). However, it will be understood that these bandwidths and distances are exemplary only and that in other embodiments greater and lesser bandwidths are possible at greater and lesser device-separation distances than given above.

[00101] Using the disclosed systems and methods, a reconfigurable communications infrastructure may be provided that allows dynamic real-time selection and interconnection of one or more individual reconfigurable signal processing circuits and/or selection and interconnection of one or more individual computing devices for executing a given computing task or computing tasks in a parallel and/or clustered manner. The reconfigurable nature of the disclosed communications infrastructure also allows for dynamic real-time re-selection of these selected reconfigurable signal processing circuits and/or individual computing devices for executing another given computing task or computing tasks in a parallel and/or clustered manner, and/or for dynamic real-time reassignment of individual reconfigurable signal processing circuits and/or individual computing devices to different computing clusters. In one embodiment, dynamic selection, reconfiguration, and interconnection may be achieved using the inter-computing device and intra-computing device capabilities of a packet router interface switch matrix ("PRISM") to route packets between each of the selected computing devices and/or between sources and destinations within the same selected computing devices in a manner as described elsewhere herein.

[00102] For example, referring to Figure 13, one or more the distributed computing devices of each of reconfigurable signal processing circuits 1310, 1314 and 1316 may be selected and configured for together performing a first computing task as a first computing cluster, while the computing device of reconfigurable signal processing circuit 1312 performs another and separate (*e.g.,* parallel) computing task or remains idle. In this regard, all of the computing devices of a given reconfigurable signal processing circuit may selected as a first computing cluster for performance of the first computing task, or only a portion of the computing devices on a given reconfigurable signal processing circuit may be selected as a first computing cluster for performing the first computing task. As an example of the latter case, FPGA device 1320 of reconfigurable signal processing circuit 1310 may be selected along with two of the FPGA devices 1320 of reconfigurable signal processing circuit 1314 and one of the FPGA devices 1320 of reconfigurable signal processing circuit 1316 as a first computing cluster for together performing the first computing task. In this case, the remaining two FPGA devices 1320

of reconfigurable signal processing circuit 1314 and the remaining FPGA device 1320 of reconfigurable signal processing circuit 1316 may be selected and configured as a second computing cluster for together performing a second computing task that may be optionally performed simultaneously and in parallel to the first computing task.

[00103] Upon completion of a given computing task (or at any other selected time), the identity of reconfigurable signal processing circuits and/or individual computing devices assigned to a given computing cluster may be optionally changed in real time. Referring to the previous example, upon completion of the first and second computing tasks, FPGA device 1320 of reconfigurable signal processing circuit 1310 may be selected along with three of the FPGA devices 1320 of reconfigurable signal processing circuit 1314 and one of the FPGA devices 1320 of reconfigurable signal processing circuit 1316 as a third computing cluster for together performing a third computing task, and the remaining FPGA device 1320 of reconfigurable signal processing circuit 1314 and the remaining FPGA device 1320 of reconfigurable signal processing circuit 1316 may be selected and configured as a fourth computing cluster for together performing a fourth computing task that may be optionally performed simultaneously and in parallel to the third computing task.

[00104] It will be understood that the above-described computing cluster examples are exemplary only and that any other suitable combination of two or more computing devices and/or two or more reconfigurable signal processing circuits may be selected for forming a computing cluster (*e.g.,* a computing cluster for performing a common computing task or tasks) and/or for performing parallel or non-parallel computing tasks. It is also possible that all of the computing devices of all of the reconfigurable signal processing circuits of a given reconfigurable communications infrastructure may be combined into a single cluster for performing a single computing task, or that each separate individual computing device of a given reconfigurable communications infrastructure may be assigned a separate and different computing task to run in parallel with the other computing devices of the given reconfigurable communications infrastructure. Thus, a variety of combinations of computing devices

and/or reconfigurable signal processing circuits are possible and dynamically reconfigurable using the disclosed systems and methods.

[00105] In the practice of the disclosed systems and methods, control for infrastructure configuration and reconfiguration (*e.g.,* assignment and reassignment of reconfigurable signal processing circuits and/or individual computing devices to given computing tasks and/or computing clusters, configuration and reconfiguration of individual computing devices for different computing tasks, *etc.*) may be provided using any suitable methodology including, but not limited to, manual control via human input of commands, automatic control via command signal received from one or more processing entities outside or within the reconfigurable communications infrastructure, combinations thereof, *etc.* For example, in one exemplary embodiment, illustrated in Figure 13, infrastructure configuration and reconfiguration may be controlled via processor node 1312. In this embodiment, the configuration of each FPGA node (1320) in the network (1350) as well as the control program for each CPU node is provided by processor node 1312. Depending on the downloaded configuration, nodes may communicate with each other or with the control processor as required. The particular configuration of the network at any given time is determined by which configurations and/or programs are loaded onto the various network elements. This configuration may be changed dynamically, if desired, to accommodate changing conditions or processing requirements.

[00106] Figure 16 illustrates a reconfigurable communications infrastructure 1300 as it may be implemented in a vehicle-based application according to one exemplary embodiment of the disclosed systems and methods. In the exemplary embodiment of Figure 16, an aircraft 1610 is shown configured with computing devices (*e.g.,* ASIC devices such as reconfigurable FPGA devices) of multiple signal processing circuits 1620 that are interconnected by a high bandwidth interconnection medium 1350 to form a reconfigurable high bandwidth network within aircraft 1610. In such an embodiment, aircraft 1610 may be a weather surveillance aircraft (manned or unmanned) and signal processing circuits 1620 may be configured for processing of data collected

from weather sensors on aircraft 1610, aircraft 1610 may be a communications aircraft (manned or unmanned) and signal processing circuits 1620 may be configured for processing (*e.g.*, demodulation, beamforming, filtering) of communications data collected from radio frequency (RF) antenna sensors on aircraft 1610, *etc.*

[00107] As shown in Figure 16, high bandwidth interconnection medium 1350 extends through bulkheads 1612 and 1614 that partition the inside of the fuselage of aircraft 1610 into multiple compartments. Thus, high bandwidth interconnection medium 1350 interconnects computing devices of signal processing circuits 1620 that are physically segregated from each other in separate compartments of aircraft 1610. In this embodiment, each of signal processing circuits 1620 may be configured, for example, in a manner as described and illustrated herein in relation to signal processing circuits 100, 1310, 1312, 1314, *etc.* In the illustrated embodiment of Figure 16, signal processing circuits 1620 have been selected to form four computing clusters 1600a, 1600b, 1600c and 1600d within aircraft 1610. In such an embodiment, each computing cluster 1600 may be configured to perform a separate computing task in parallel or non-parallel manner with the other computing clusters.

[00108] Figure 17 illustrates how vehicle-based reconfigurable communications infrastructure 1300 of Figure 16 may be reconfigured (*e.g.*, dynamically reconfigured during in-flight operations of aircraft 1610) so that signal processing circuits have been selected to form two computing clusters 1600e and 1600f within aircraft 1610. Once again, each computing cluster 1600e and 1600f may be configured to perform a separate computing task in parallel or non-parallel manner with the other computing clusters.

[00109] Figure 18 illustrates a reconfigurable communications infrastructure 1300 as it may be implemented in a vehicle-based application according to another exemplary embodiment of the disclosed systems and methods. In the exemplary embodiment of Figure 18, a seismic data collection trailer 1812 and a seismic data processing truck 1814 is each shown configured with computing devices (*e.g.*, ASIC

devices such as reconfigurable FPGA devices) of multiple signal processing circuits 1820 that are interconnected by a high bandwidth interconnection medium 1350 to form a reconfigurable high bandwidth network.

[00110] As shown in Figure 18, high bandwidth interconnection medium 1350 extends between truck 1814 and trailer 1812 so as to interconnect computing devices of signal processing circuits 1820 that are physically segregated from each other in separate vehicles. In this embodiment, each of signal processing circuits 1820 may be configured, for example, in a manner as described and illustrated herein in relation to signal processing circuits 100, 1310, 1312, 1314, *etc.* In the embodiment illustrated in Figure 18, signal processing circuits 1820 have been selected to form a single computing cluster 1700, *e.g.,* for collection and parallel processing of large amounts of data from geophones 1810 (*e.g.,* using matrix arithmetic and with each of signal processing circuits 1820 processing data in parallel to the other signal processing circuits 1820) for multi-dimensional reconstruction of this collected data in the field.

[00111] It will be understood that the embodiments of Figures 16-18 are exemplary only and that multiple computing devices may be interconnected in a manner suitable for forming a reconfigurable communications infrastructure for use in any other suitable processing environment (*e.g.,* other type of vehicle/s or building/s, *etc.*), and/or in manner suitable to perform other types of signal processing application/s.

[00112] While the invention may be adaptable to various modifications and alternative forms, specific embodiments have been shown by way of example and described herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims. Moreover, the different aspects of the disclosed systems and methods may be utilized in various combinations and/or independently. Thus the invention is not limited to only those combinations shown herein, but rather may include other combinations.

WHAT IS CLAIMED IS:

1. A method, comprising:

providing two or more ASIC devices, each one of said two or more ASIC devices comprising a packet router;

providing a high bandwidth interconnection medium coupled between said packet routers of each of said two or more ASIC devices to form a reconfigurable communications infrastructure; and

communicating data between said packet routers of each of said two or more ASIC devices across said high bandwidth interconnection medium.

2. The method of claim 1, wherein each of said two or more ASIC devices comprises FPGA devices.

3. The method of claim 2, further comprising:

providing said two or more FPGA devices by providing two or more signal processing circuits, each one of said two or more signal processing circuits comprising at least one FPGA device that comprises a packet router;

providing said high bandwidth interconnection medium coupled between said two or more signal processing circuits to provide data communication between said packet routers of said FPGA devices of each of said two or more signal processing circuits; and

communicating data across said high bandwidth interconnection medium between said packet routers of said FPGA devices of each of said two or more signal processing circuits.

4. The method of claim 3, wherein at least one of said signal processing circuits is a reconfigurable signal processing circuit that further comprises two or more FPGA devices that each comprise a packet router, said packet router of each one of said two or more FPGA devices of said at least one signal processing circuit being coupled to each respective packet router of each of the other of said two or more FPGA devices of said at least one signal processing circuit; and wherein said method further comprises using said packet router of each given one of said two or more FPGA devices of said at least one signal processing circuit to communicate data packets with each other of said two or more FPGA devices of said at least one signal processing circuit.

5. The method of claim 4, wherein said packet router of each one of said two or more FPGA devices of said at least one signal processing circuit is coupled to each respective packet router of each of the other of said two or more FPGA devices of said at least one signal processing circuit by a separate respective duplex data communication link so as to form a direct serial interconnection between each two of said two or more FPGA devices of said signal processing circuit; and wherein said method further comprises using said packet router of each given one of said two or more FPGA devices of said at least one signal processing circuit to transmit and receive data packets across each of said separate respective duplex data communication links existing between said given one of said two or more FPGA devices and each other of said two or more FPGA devices of said at least one signal processing circuit.

6. The method of claim 2, wherein each given one of said two or more FPGA devices comprises user-defined circuitry coupled to said respective packet router of said

given one of said two or more FPGA devices; and wherein said method further comprises transmitting and receiving data packets between said user-defined circuitry of said given one of said two or more FPGA devices and said high bandwidth interconnection medium.

7. The method of claim 2, wherein each given one of said two or more FPGA devices comprises at least one embedded processor coupled to said respective packet router of said given one of said two or more FPGA devices; and wherein said method further comprises transmitting and receiving data packets between said at least one embedded processor of said given one of said two or more FPGA devices and said high bandwidth interconnection medium.

8. The method of claim 2, further comprising providing a vehicle-based reconfigurable communications infrastructure comprising a vehicle with each of said two or more FPGA devices and said high bandwidth interconnection medium being positioned on or within said vehicle; and communicating data between said packet routers of each of said two or more FPGA devices across said high bandwidth interconnection medium on or within said vehicle.

9. The method of claim 2, further comprising providing said two or more FPGA devices in positions physically segregated from each other; and communicating data between said packet routers of each of said two or more physically-segregated FPGA devices across said high bandwidth interconnection medium.

10. The method of claim 2, wherein said high bandwidth interconnection medium comprises an optical transmission medium; and wherein said method further comprises communicating data between said packet routers of each of said two or more FPGA devices across said optical transmission medium.

11. The method of claim 2, further comprising communicating data between said packet routers of each of said two or more FPGA devices at a data transmission rate of greater than or equal to about 1 Gbps.

12. The method of claim 2, further comprising configuring each of said at least two FPGA devices to perform different computing tasks in parallel.

13. The method of claim 2, further comprising:

providing said two or more FPGA devices as first and second FPGA devices;

configuring said first and second FPGA devices to perform a first computing task together as a first computing cluster;

providing at least two additional FPGA devices as third and fourth FPGA devices, each one of said third and fourth FPGA devices comprising a packet router coupled to said high bandwidth interconnection medium;

configuring said third and fourth FPGA devices to perform a second computing task together as a second computing cluster, said second computing task being different than said first computing task; and

simultaneously performing said first computing task with said first computing cluster and said second computing task with said second computing cluster.

14. The method of claim 13, further comprising:

reconfiguring said first and third FPGA devices to perform a third computing task together as a third computing cluster;

configuring said second and fourth FPGA devices to perform a fourth computing task together as a fourth computing cluster, said fourth computing task being different than said third computing task; and

simultaneously performing said third computing task with said third computing cluster and said fourth computing task with said fourth computing cluster.

15. The method of claim 13, further comprising:

reconfiguring said first, second, third and fourth FPGA devices to perform a third computing task together as a third computing cluster; and

performing said third computing task with said third computing.

16. A reconfigurable communications infrastructure, comprising:

two or more ASIC devices, each one of said two or more ASIC devices comprising a packet router; and

a high bandwidth interconnection medium coupled between said packet routers of each of said two or more ASIC devices to provide data communication between said packet routers of each of said two or more ASIC devices.

17. The reconfigurable communications infrastructure of claim 16, wherein each of said two or more ASIC devices comprises FPGA devices.

18. The reconfigurable communications infrastructure of claim 17, further comprising:

two or more signal processing circuits, each one of said two or more signal processing circuits comprising at least one FPGA device that comprises a packet router; and

wherein said high bandwidth interconnection medium is coupled between said two or more signal processing circuits to provide data communication between said packet routers of said FPGA devices of each of said two or more signal processing circuits.

19. The reconfigurable communications infrastructure of claim 18, wherein at least one of said signal processing circuits is a reconfigurable signal processing circuit that further comprises two or more FPGA devices that each comprise a packet router, said packet router of each one of said two or more FPGA devices of said at least one signal processing circuit being coupled to each respective packet router of each of the other of said two or more FPGA devices of said at least one signal processing circuit.

20. The reconfigurable communications infrastructure of claim 19, wherein said packet router of each one of said two or more FPGA devices of said at least one signal processing circuit is coupled to each respective packet router of each of the other of said two or more FPGA devices of said at least one signal processing circuit by a separate respective duplex data communication link so as to form a direct serial interconnection between each two of said two or more FPGA devices of said signal processing circuit.

21. The reconfigurable communications infrastructure of claim 17, wherein each given one of said two or more FPGA devices comprises user-defined circuitry coupled to said respective packet router of said given one of said two or more FPGA devices; and wherein said respective packet router of each given one of said two or more FPGA devices is configured to transmit and receive data packets between said user-defined circuitry of said given one of said two or more FPGA devices and said high bandwidth interconnection medium.

22. The reconfigurable communications infrastructure of claim 17, wherein each given one of said two or more FPGA devices comprises at least one embedded processor coupled to said respective packet router of said given one of said two or more FPGA devices; and wherein said respective packet router of each given one of said two or more FPGA devices is configured to transmit and receive data packets between said at least one embedded processor of said given one of said two or more FPGA devices and said high bandwidth interconnection medium.

23. The reconfigurable communications infrastructure of claim 17, wherein said reconfigurable communications infrastructure is a vehicle-based reconfigurable communications infrastructure comprising a vehicle; and wherein each of said two or more FPGA devices is positioned on or within said vehicle.

24. The reconfigurable communications infrastructure of claim 17, wherein said two or more FPGA devices are physically segregated from each other.

25. The reconfigurable communications infrastructure of claim 17, wherein said high bandwidth interconnection medium comprises an optical transmission medium.

26. The reconfigurable communications infrastructure of claim 17, wherein said high bandwidth interconnection medium comprises an interconnection medium having a data transmission capability of greater than or equal to about 1 Gbps.

27. A communications infrastructure, comprising two or more ASIC devices, each one of said two or more ASIC devices comprising a packet router, said packet router of each one of said two or more ASIC devices being coupled to each respective packet router of each of the other of said two or more ASIC devices by an interconnection comprising a high speed serial optical link.

28. The communications infrastructure of claim 27, wherein said interconnection further comprises a high bandwidth interconnection medium.

29. The communications infrastructure of claim 28, wherein each of said two or more ASIC devices comprises FPGA devices.

30. The communications infrastructure of claim 29, further comprising:

two or more signal processing circuits, each one of said two or more signal processing circuits comprising at least one FPGA device that comprises a packet router; and

wherein said interconnection is coupled between said two or more signal processing circuits to provide data communication between said packet routers of said FPGA devices of each of said two or more signal processing circuits.

31. A method, comprising:

providing two or more ASIC devices, each one of said two or more ASIC devices comprising a packet router coupled together by an interconnection comprising a high speed serial optical link, and

transferring at least one data packet from each said packet router of each one of said two or more ASIC devices to each respective packet router of each of the other of said two or more ASIC devices by said high speed serial optical link.

32. The method of claim 31, wherein said interconnection further comprises a high bandwidth interconnection medium.

33. The method of claim 32, wherein each of said two or more ASIC devices comprises FPGA devices.

34. The method of claim 33, further comprising:

providing said two or more FPGA devices by providing two or more signal processing circuits, each one of said two or more signal processing

circuits comprising at least one FPGA device that comprises a packet router;

providing said interconnection coupled between said two or more signal processing circuits to provide data communication between said packet routers of said FPGA devices of each of said two or more signal processing circuits; and

communicating data across said interconnection between said packet routers of said FPGA devices of each of said two or more signal processing circuits.

ABSTRACT

Reconfigurable communications infrastructures may be implemented to interconnect ASIC devices (*e.g.,* FPGAs) and other computing and input/output devices using high bandwidth interconnection mediums. The computing and input/output devices may be positioned in locations that are physically segregated from each other, and/or may be provided to project a reconfigurable network across a wide area. The reconfigurable communications infrastructures may be implemented to allow such computing and input/output devices to be used in different arrangements and applications, *e.g.,* for use in any application where a large array of ASIC devices may be usefully employed such as supercomputing, *etc.*

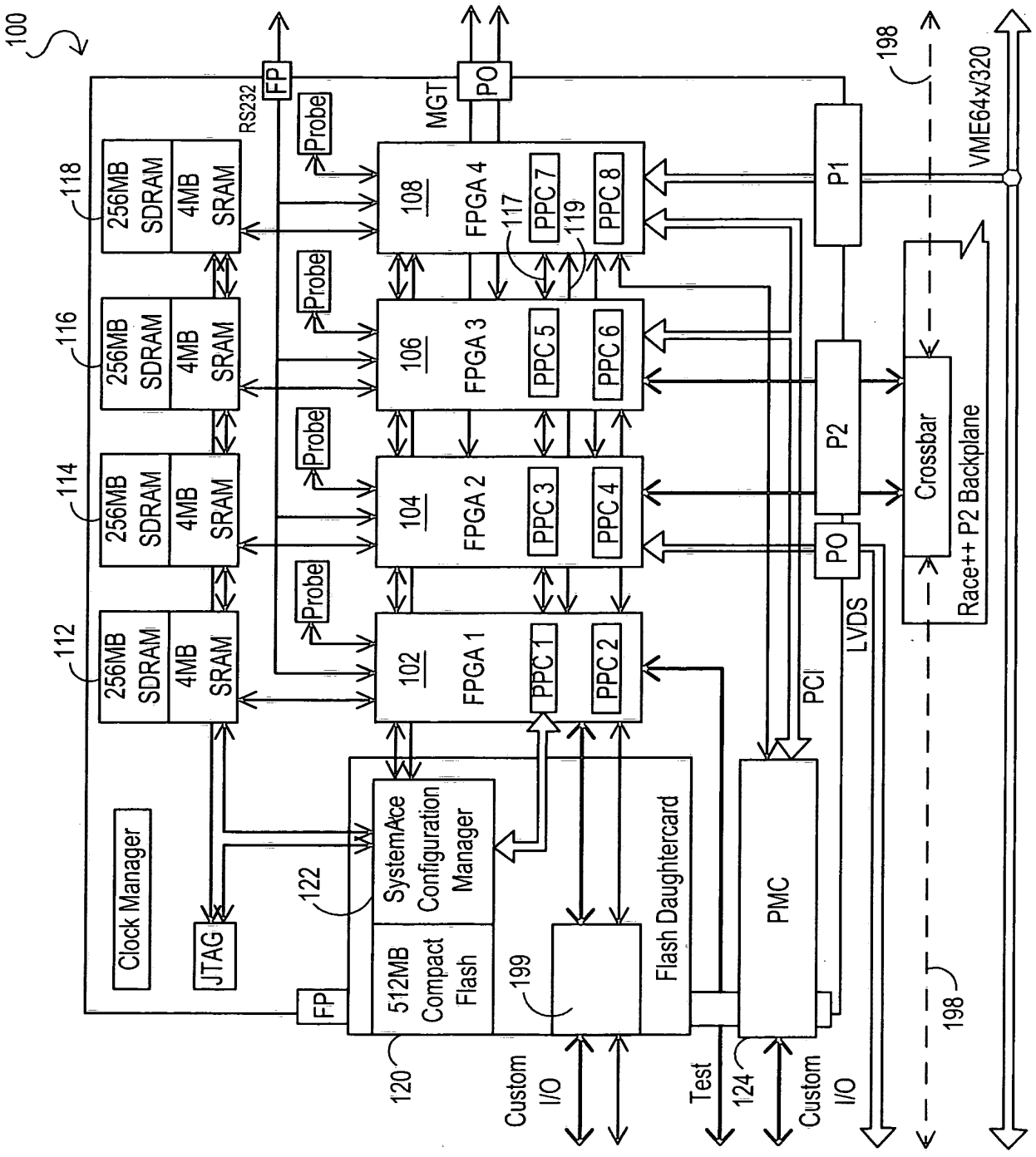

100
FP
RS232
Probe
MGT
PO
198
VME64x/320
118
256MB SDRAM
4MB SRAM
108
FPGA 4
117
PPC 7
119
PPC 8
P1
116
106
FPGA 3
PPC 5
PPC 6
P2
Crossbar
114
104
FPGA 2
PPC 3
PPC 4
Race++ P2 Backplane
112
102
FPGA 1
PPC 1
PPC 2
LVDS
PCI
Clock Manager
JTAG
122
SystemAce Configuration Manager
512MB Compact Flash
199
Flash Daughtercard
PMC
120
Custom I/O
Test
124
Custom I/O

FIG. 1

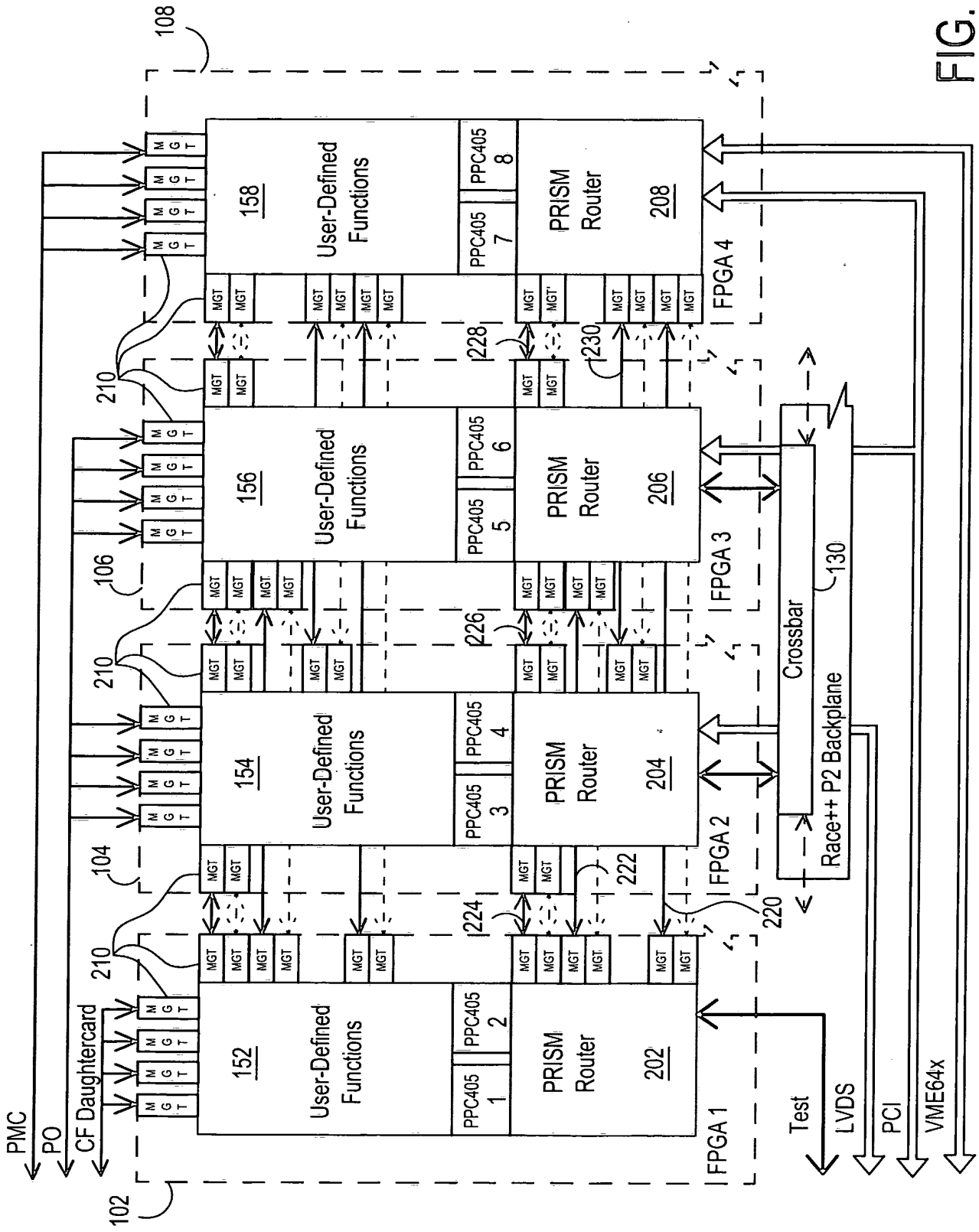

108
158
User-Defined Functions
PPC405 8
PPC405 7
PRISM Router
208
FPGA 4
156
User-Defined Functions
PPC405 6
PPC405 5
PRISM Router
206
FPGA 3
154
User-Defined Functions
PPC405 4
PPC405 3
PRISM Router
204
FPGA 2
152
User-Defined Functions
PPC405 2
PPC405 1
PRISM Router
202
FPGA 1
MGT
210
228
230
226
224
222
220
106
104
102
Crossbar
130
Race++ P2 Backplane
PMC
PO
CF Daughtercard
Test
LVDS
PCI
VME64x

FIG. 2

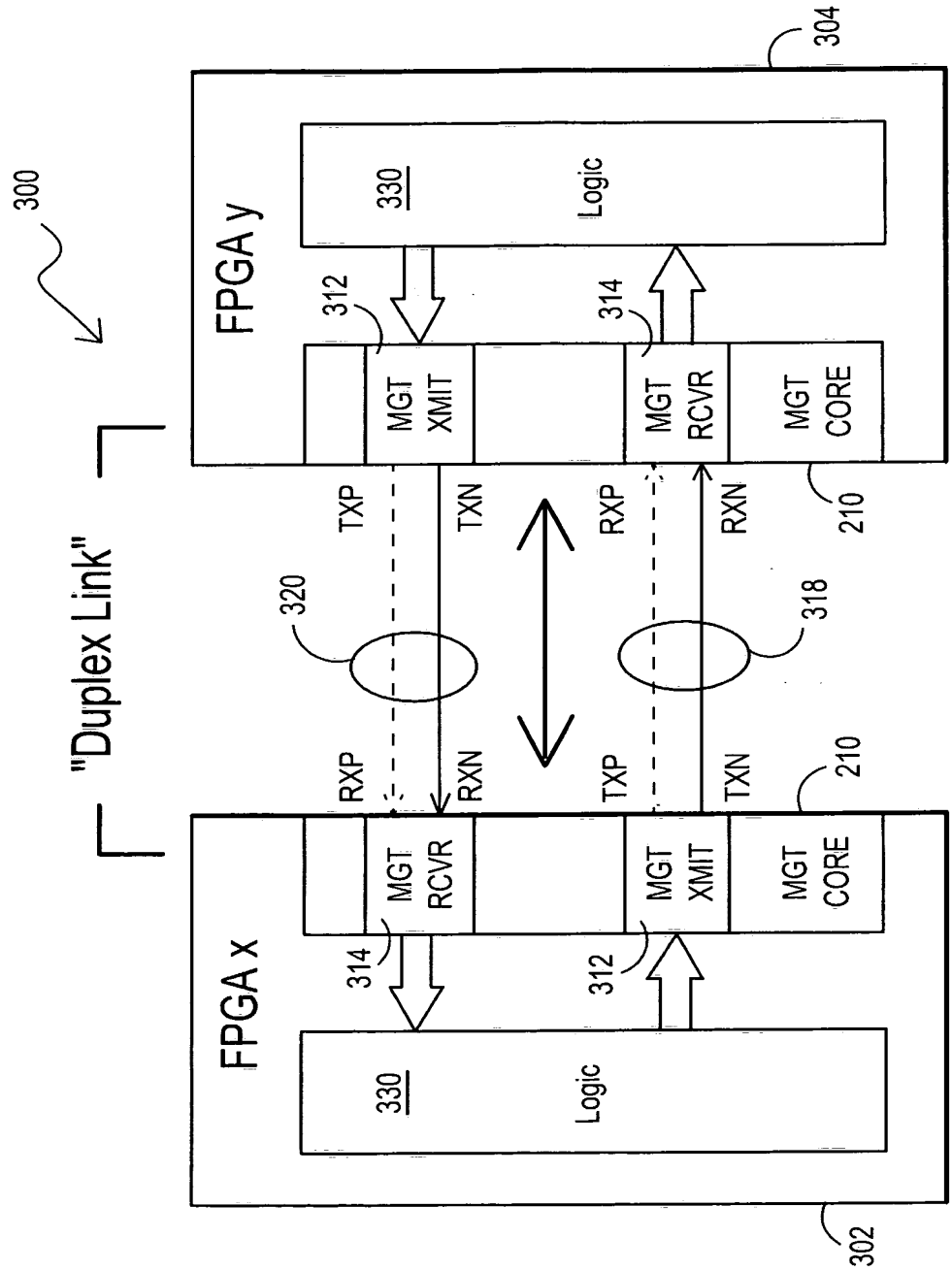

300
"Duplex Link"
FPGA y
FPGA x
304
302
330
Logic
312
314
MGT XMIT
MGT RCVR
MGT CORE
210
TXP
TXN
RXP
RXN
320
318

FIG. 3

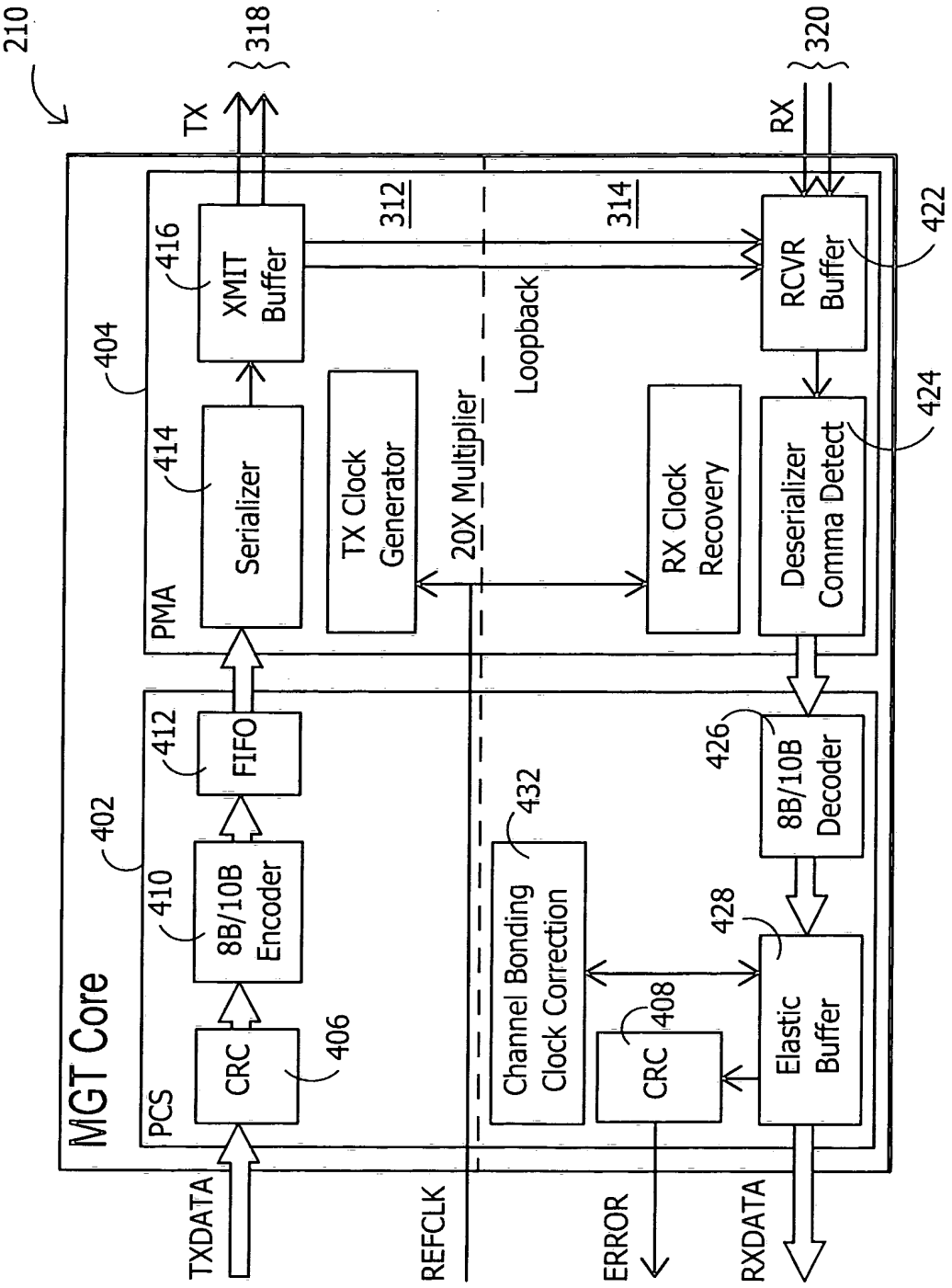

210
TX
318
RX
320
MGT Core
PCS
PMA
402
404
406
CRC
408
CRC
410
8B/10B Encoder
412
FIFO
414
Serializer
416
XMIT Buffer
312
314
Loopback
RCVR Buffer
422
424
Deserializer Comma Detect
426
8B/10B Decoder
428
Elastic Buffer
432
Channel Bonding Clock Correction
20X Multiplier
TX Clock Generator
RX Clock Recovery
TXDATA
REFCLK
ERROR
RXDATA

FIG. 4

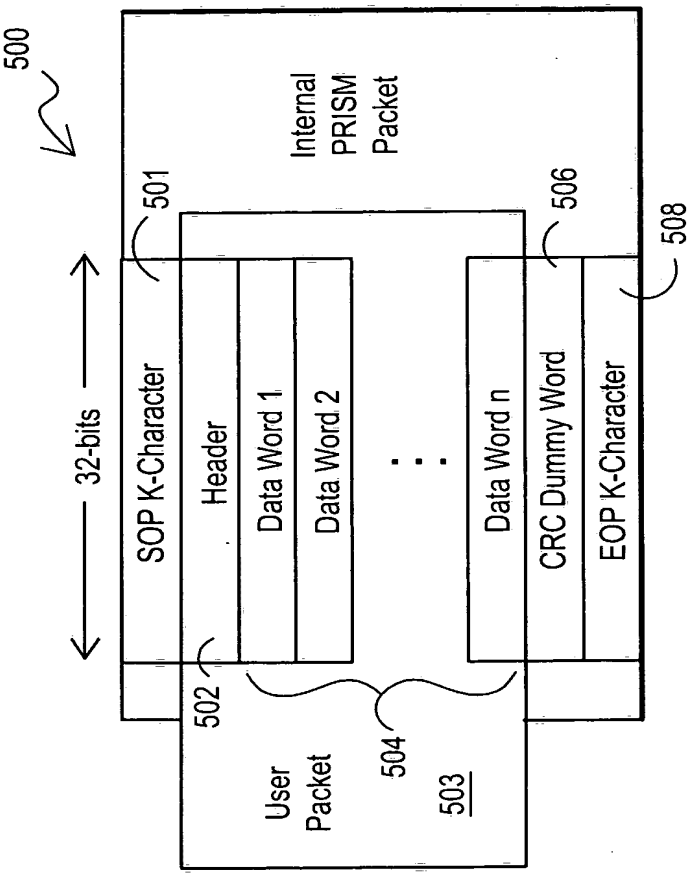

500
Internal PRISM Packet
501
506
508
32-bits
SOP K-Character
Header
Data Word 1
Data Word 2
Data Word n
CRC Dummy Word
EOP K-Character
502
504
User Packet
503

FIG. 5

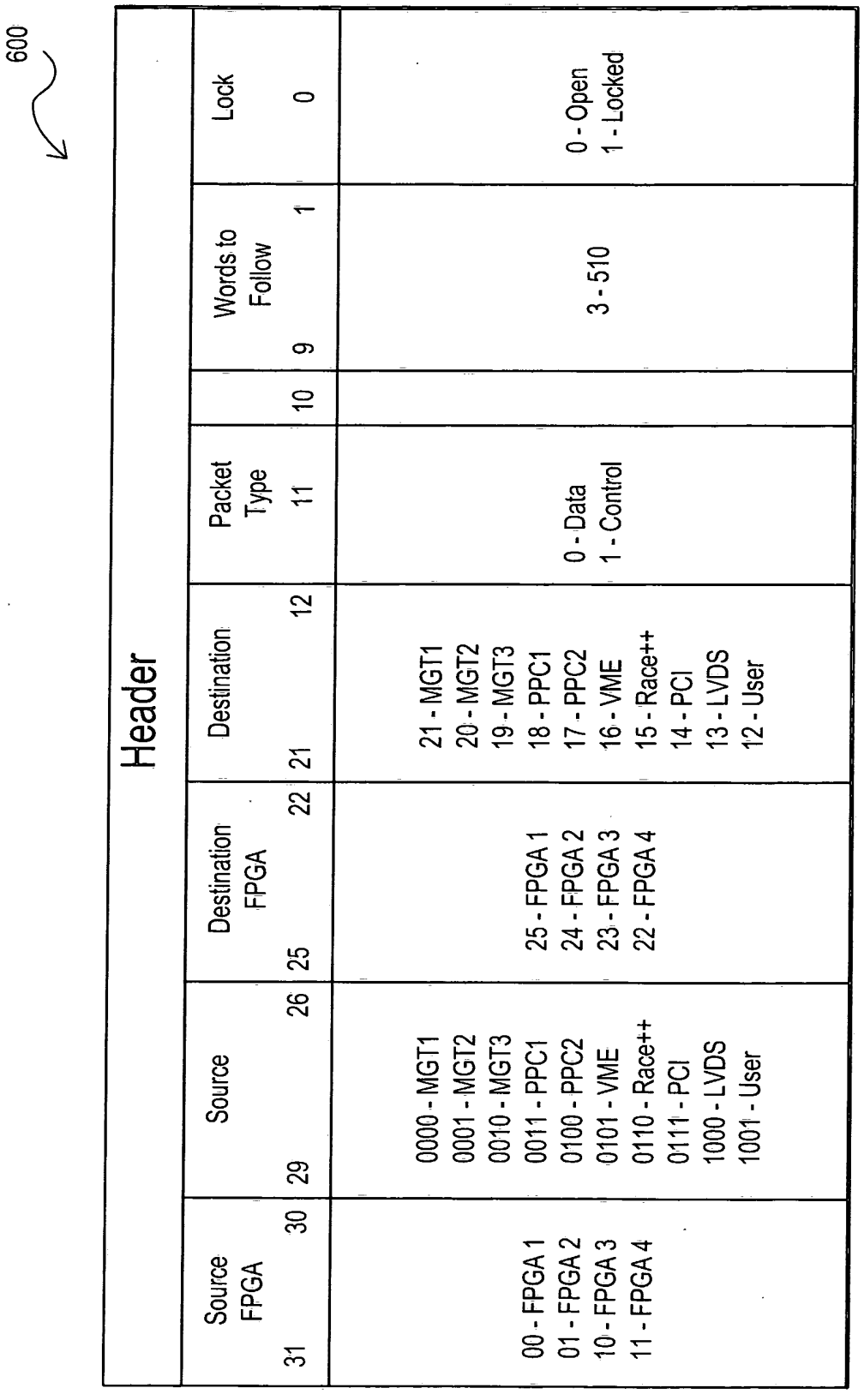

600
Header
Source FPGA
31 30
Source
29 26
Destination FPGA
25 22
Destination
21 12
Packet Type
11
10
Words to Follow
9 1
Lock
0
0000 - MGT1
0001 - MGT2
0010 - MGT3
0011 - PPC1
0100 - PPC2
0101 - VME
0110 - Race++
0111 - PCI
1000 - LVDS
1001 - User
00 - FPGA 1
01 - FPGA 2
10 - FPGA 3
11 - FPGA 4
25 - FPGA 1
24 - FPGA 2
23 - FPGA 3
22 - FPGA 4
21 - MGT1
20 - MGT2
19 - MGT3
18 - PPC1
17 - PPC2
16 - VME
15 - Race++
14 - PCI
13 - LVDS
12 - User
0 - Data
1 - Control
3 - 510
0 - Open
1 - Locked

FIG. 6

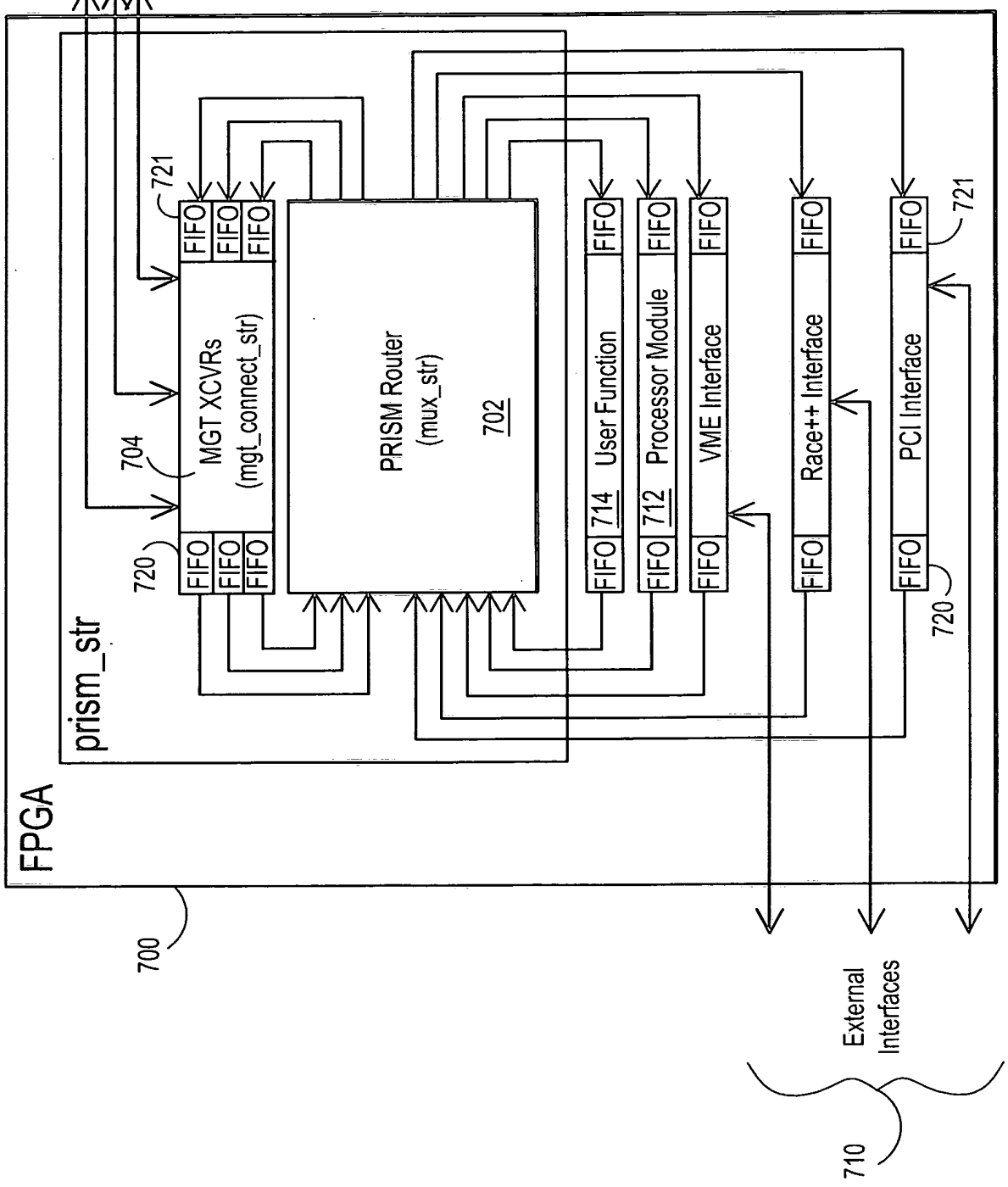

Other FPGAs
FPGA
prism_str
700
721
FIFO
MGT XCVRs (mgt_connect_str)
704
720
PRISM Router (mux_str)
702
User Function
714
Processor Module
712
VME Interface
Race++ Interface
PCI Interface
External Interfaces
710

FIG. 7

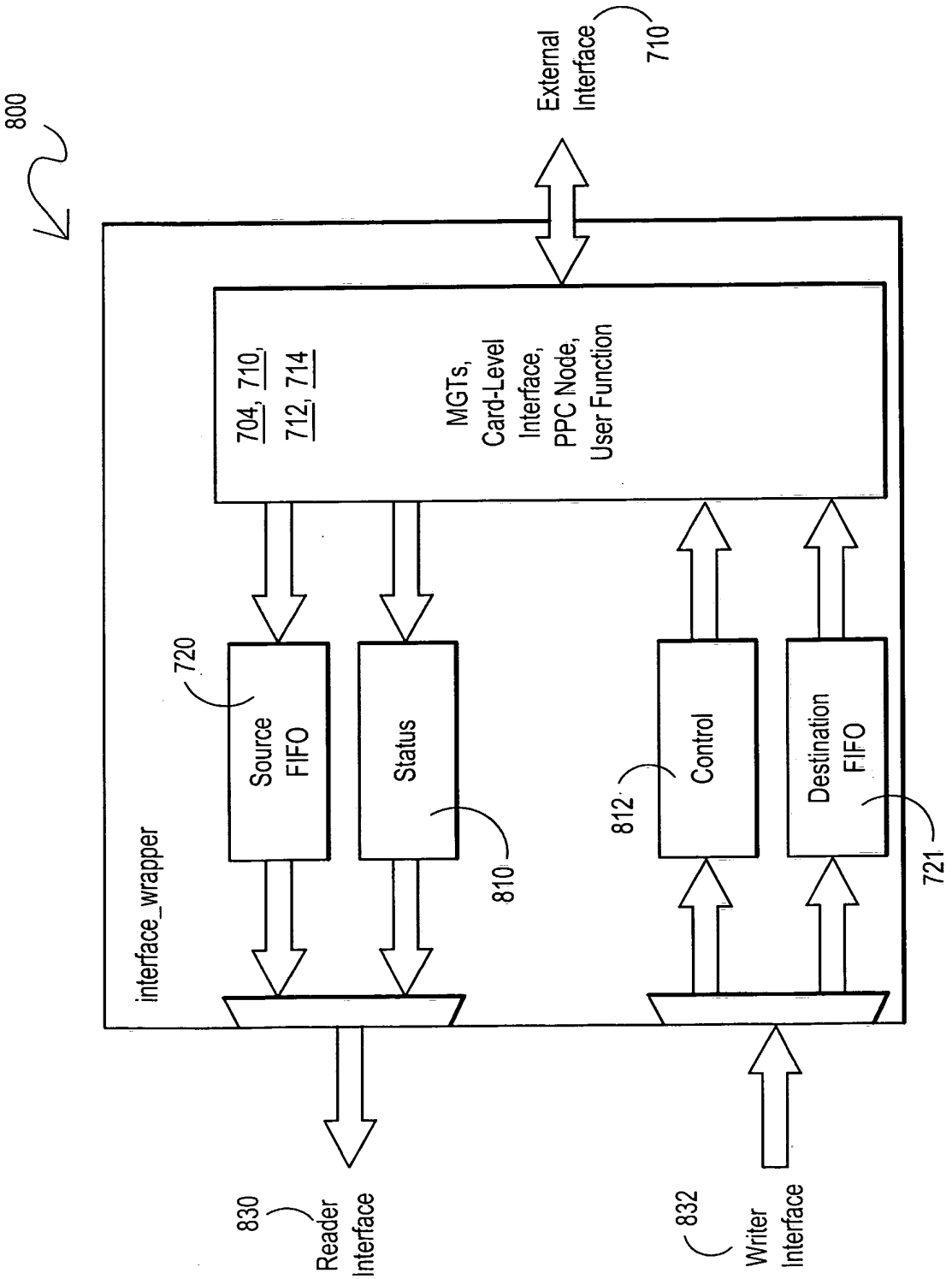

800
External Interface
710
704, 710, 712, 714
MGTs, Card-Level Interface, PPC Node, User Function
720
Source FIFO
Status
810
812
Control
Destination FIFO
721
interface_wrapper
830
Reader Interface
832
Writer Interface

FIG. 8

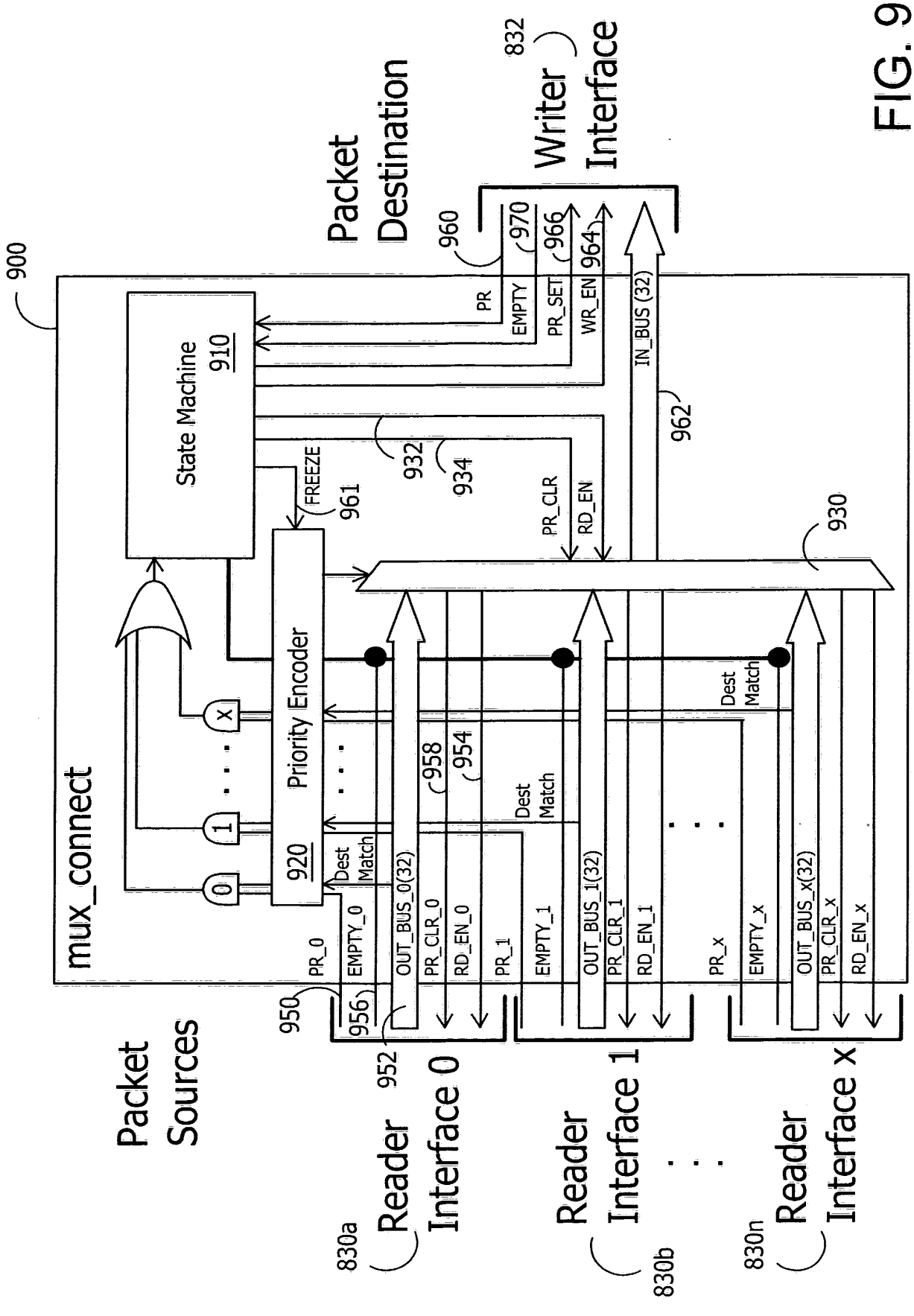

900
mux_connect
State Machine
910
Priority Encoder
920
930
Packet Destination
960
Writer Interface
832
PR
EMPTY
PR_SET
WR_EN
IN_BUS (32)
962
970
966
964
FREEZE
961
932
934
PR_CLR
RD_EN
Dest Match
958
954
956
952
950
PR_0
EMPTY_0
OUT_BUS_0(32)
PR_CLR_0
RD_EN_0
PR_1
EMPTY_1
OUT_BUS_1(32)
PR_CLR_1
RD_EN_1
PR_x
EMPTY_x
OUT_BUS_x(32)
PR_CLR_x
RD_EN_x
0
1
x
Packet Sources
Reader Interface 0
830a
Reader Interface 1
830b
Reader Interface x
830n

FIG. 9

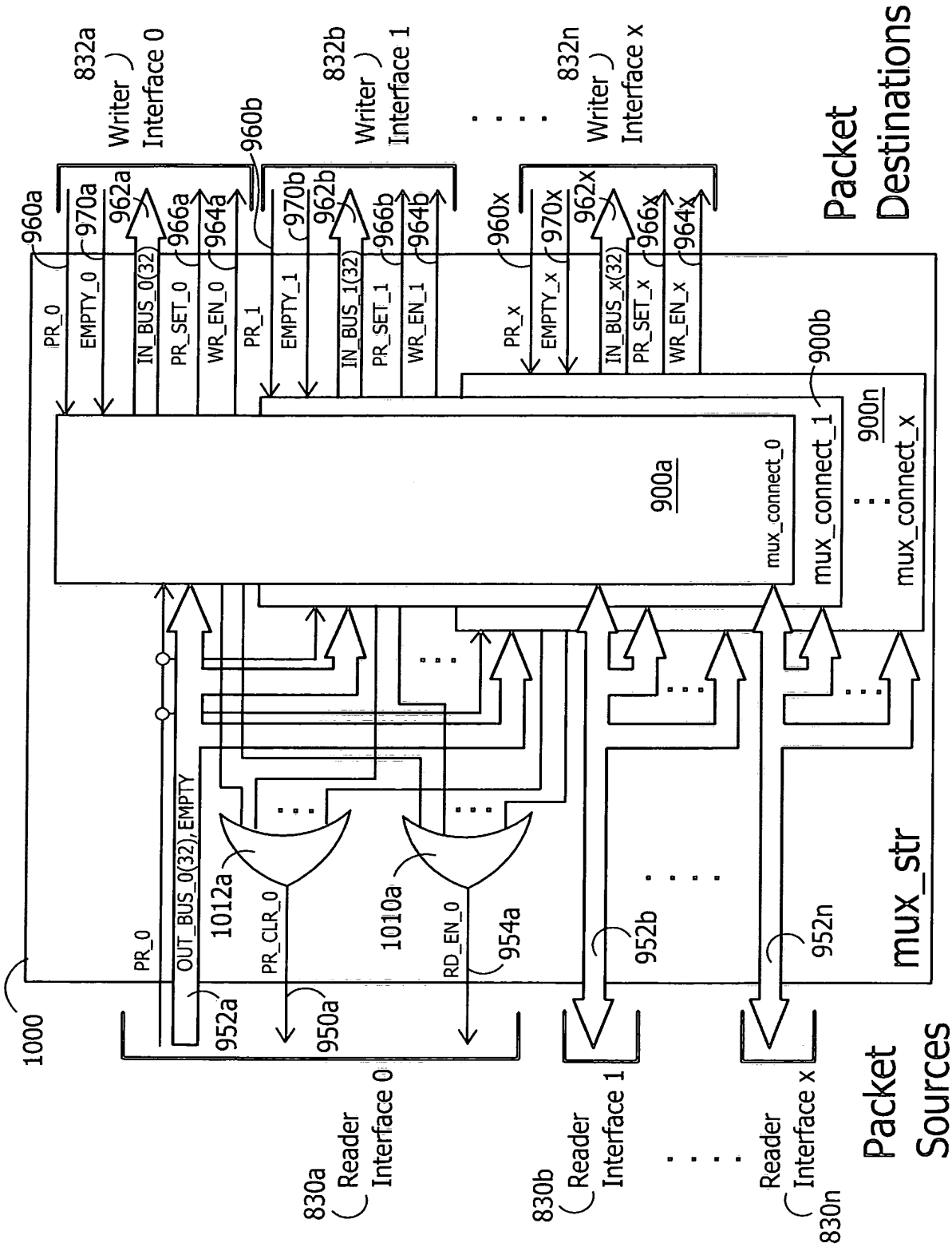

Packet Destinations
Packet Sources
mux_str
1000
832a Writer Interface 0
832b Writer Interface 1
832n Writer Interface x
960a
960b
960x
970a
962a
966a
964a
970b
962b
966b
964b
970x
962x
966x
964x
PR_0
EMPTY_0
IN_BUS_0(32)
PR_SET_0
WR_EN_0
PR_1
EMPTY_1
IN_BUS_1(32)
PR_SET_1
WR_EN_1
PR_x
EMPTY_x
IN_BUS_x(32)
PR_SET_x
WR_EN_x
900a
900b
900n
mux_connect_0
mux_connect_1
mux_connect_x
OUT_BUS_0(32),EMPTY
1012a
PR_CLR_0
1010a
RD_EN_0
954a
952a
950a
952b
952n
830a Reader Interface 0
830b Reader Interface 1
Reader Interface x
830n

FIG. 10

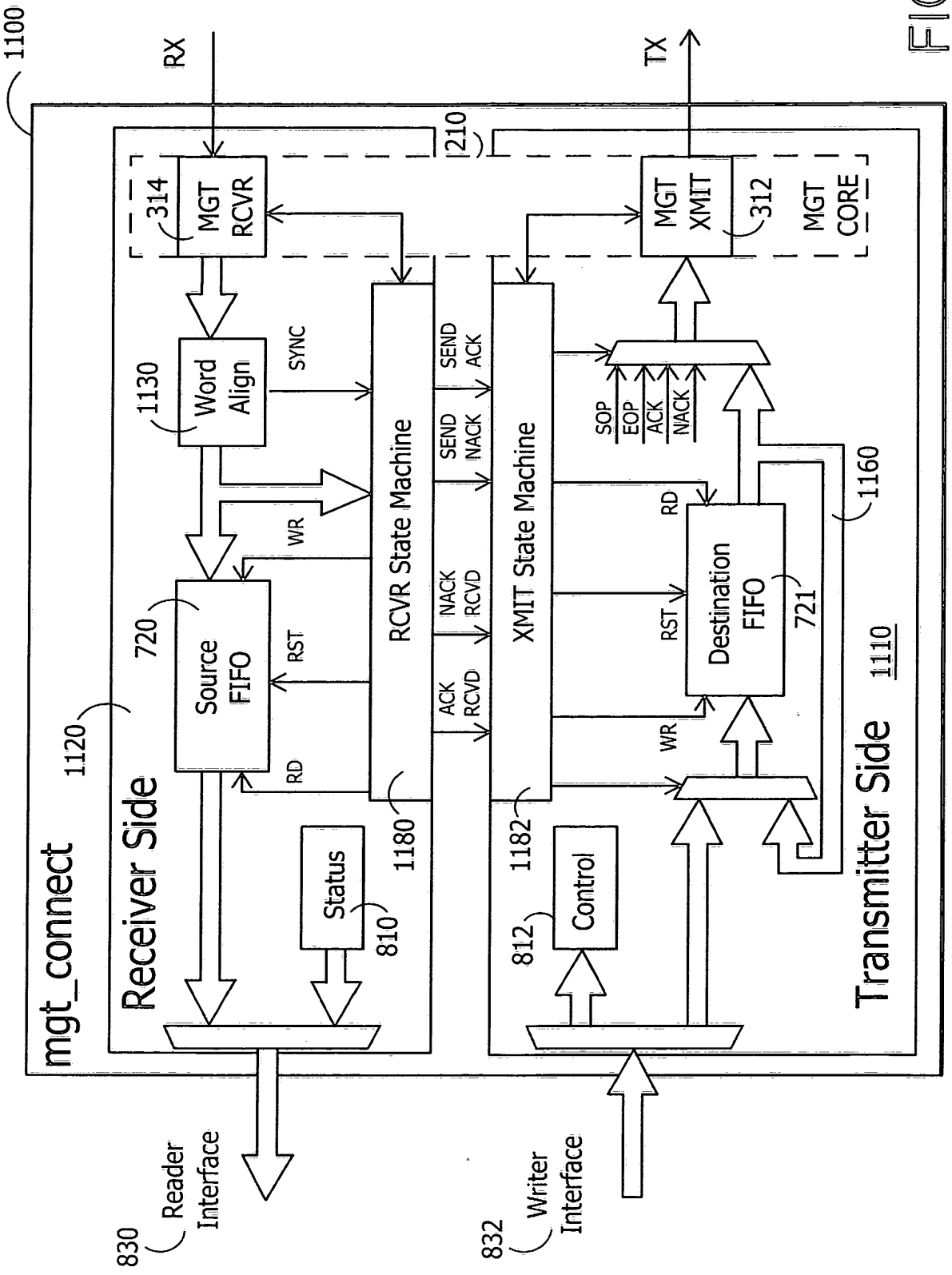

1100
RX
TX
210
314
MGT RCVR
MGT XMIT
312
MGT CORE
1130
Word Align
SYNC
SEND ACK
SEND NACK
NACK RCVD
ACK RCVD
RCVR State Machine
XMIT State Machine
SOP
EOP
ACK
NACK
RD
WR
RST
720
Source FIFO
Destination FIFO
721
1160
1120
Receiver Side
1110
Transmitter Side
mgt_connect
Status
810
1180
1182
812
Control
830
Reader Interface
832
Writer Interface

FIG. 11

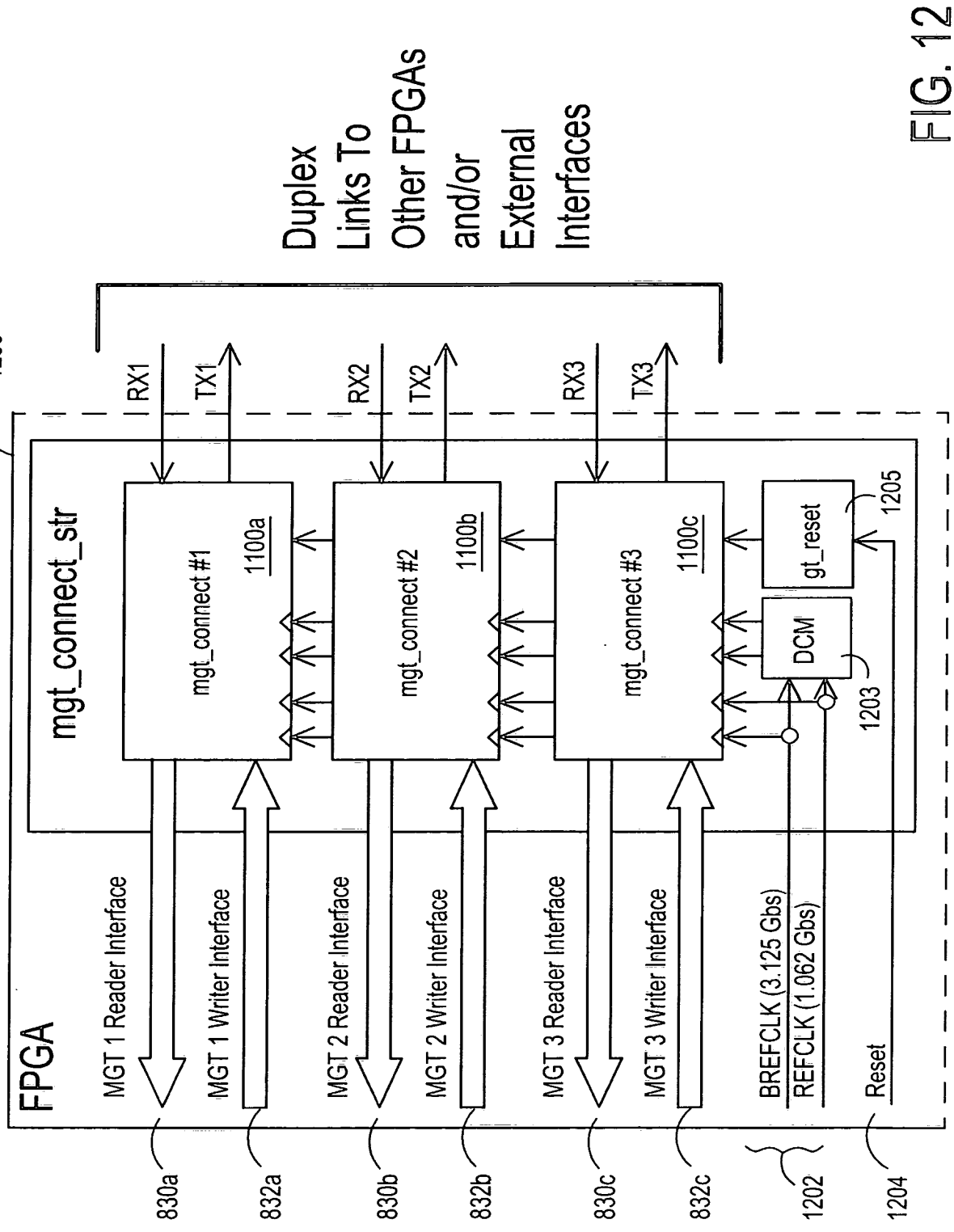

Duplex Links To Other FPGAs and/or External Interfaces
1200
FPGA
mgt_connect_str
RX1
TX1
RX2
TX2
RX3
TX3
mgt_connect #1
1100a
mgt_connect #2
1100b
mgt_connect #3
1100c
gt_reset
1205
DCM
1203
MGT 1 Reader Interface
MGT 1 Writer Interface
MGT 2 Reader Interface
MGT 2 Writer Interface
MGT 3 Reader Interface
MGT 3 Writer Interface
BREFCLK (3.125 Gbs)
REFCLK (1.062 Gbs)
Reset
830a
832a
830b
832b
830c
832c
1202
1204

FIG. 12

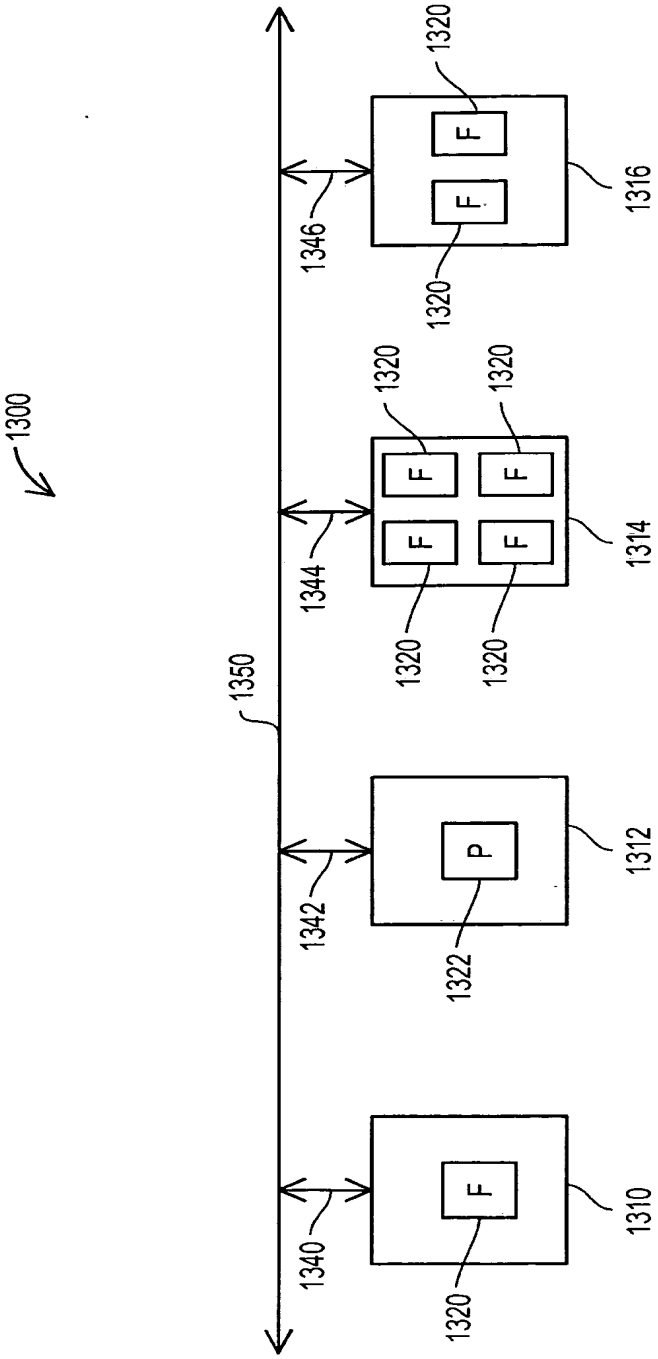

1300
1350
1310
1312
1314
1316
1320
1322
1340
1342
1344
1346
F
P

FIG. 13

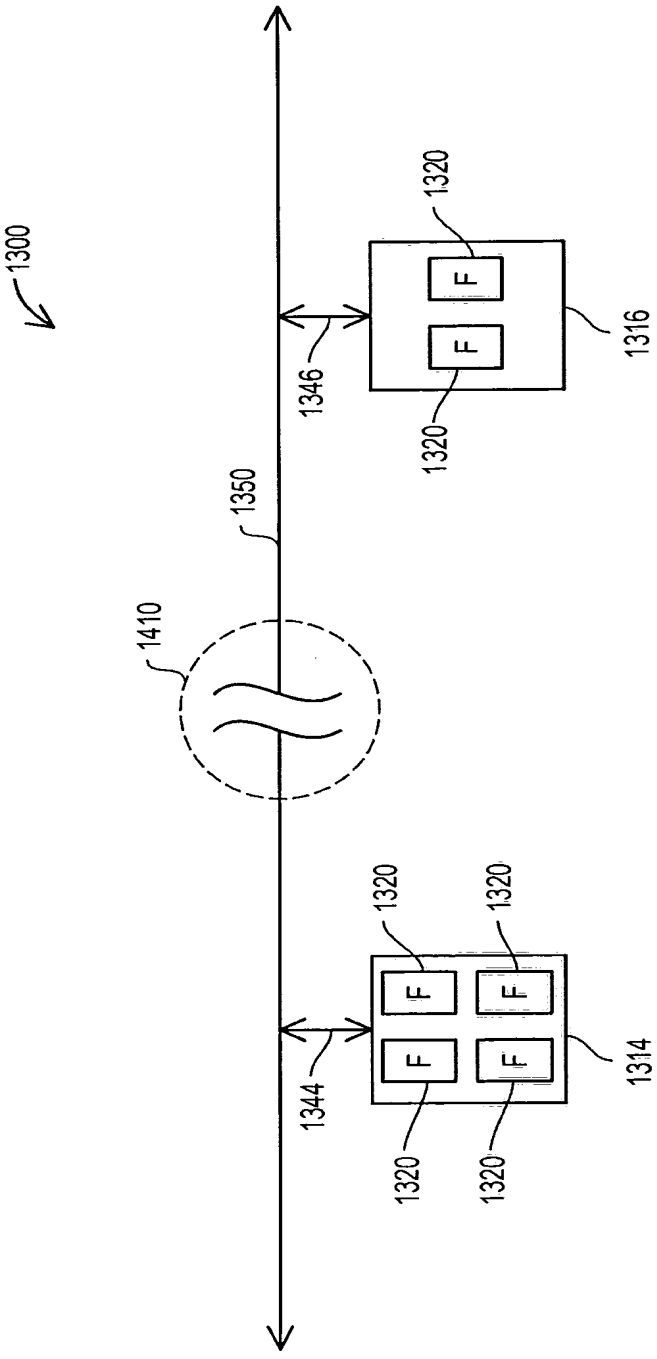

1300
1320
F
F
1316
1346
1320
1350
1410
1320
1320
F
F
F
F
1314
1344
1320
1320

FIG. 14

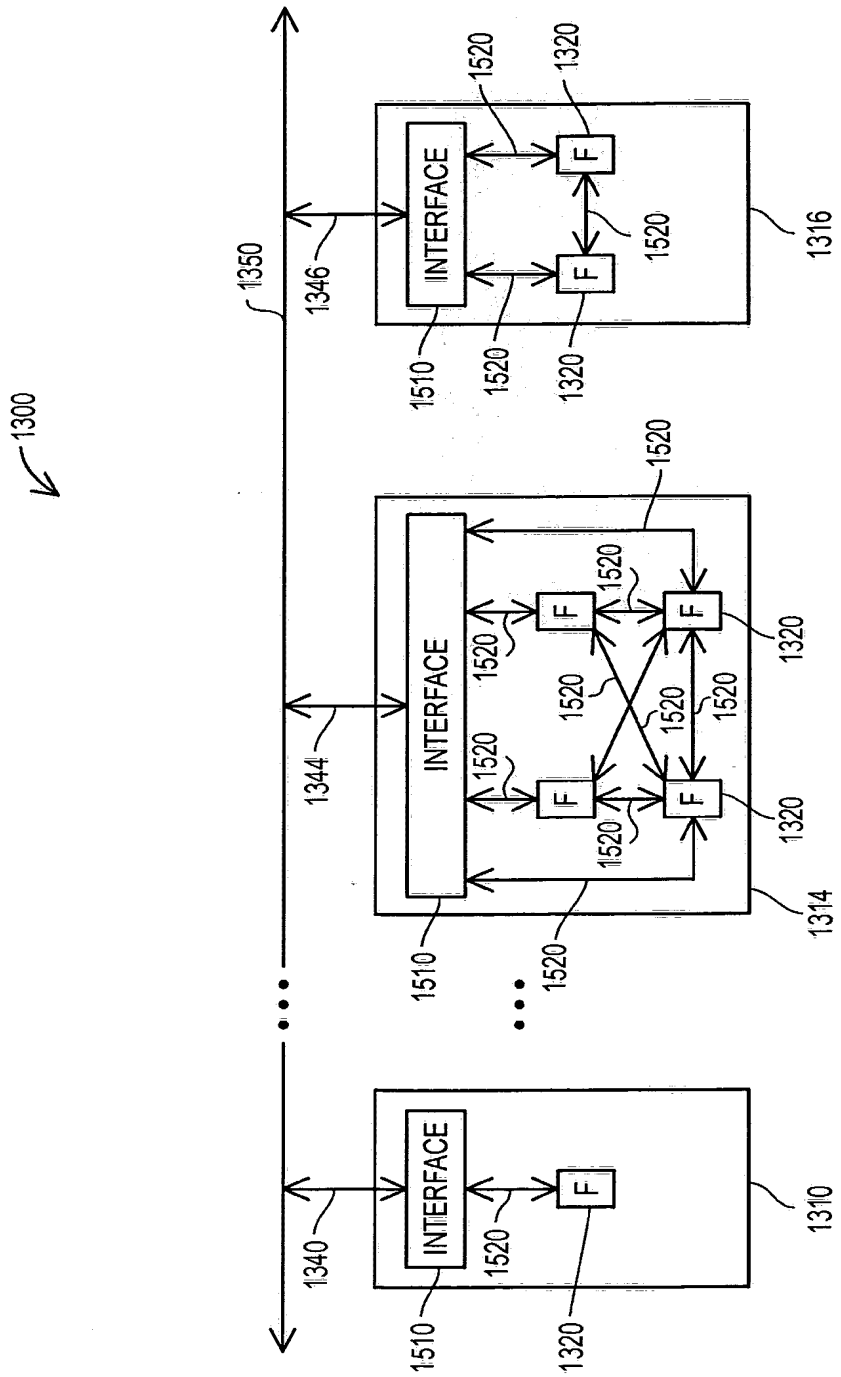

1300
1350
1346
1344
1340
INTERFACE
F
1520
1320
1510
1316
1314
1310

FIG. 15

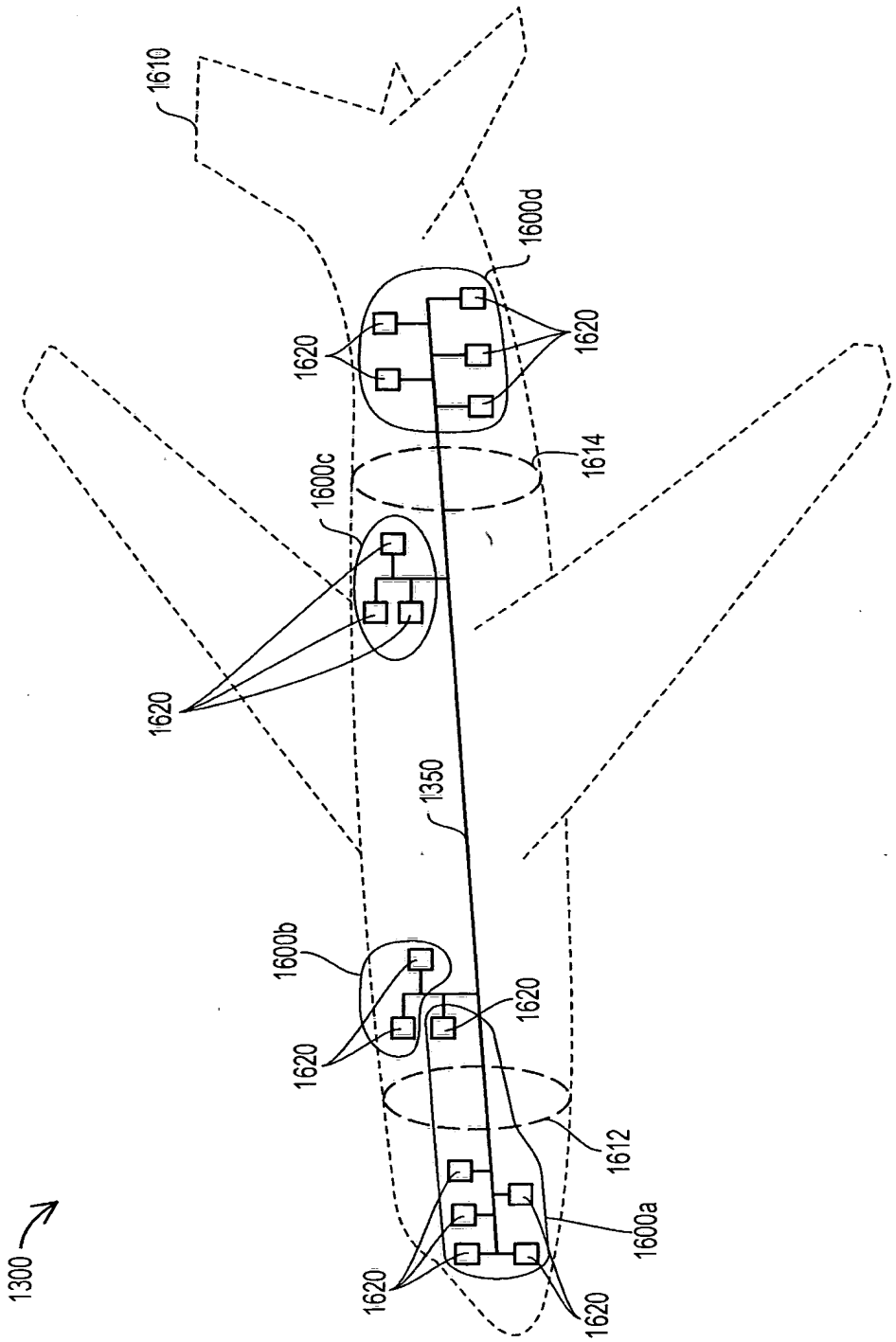

1610
1600d
1620
1620
1614
1600c
1620
1350
1600b
1620
1620
1612
1600a
1620
1620
1300

FIG. 16

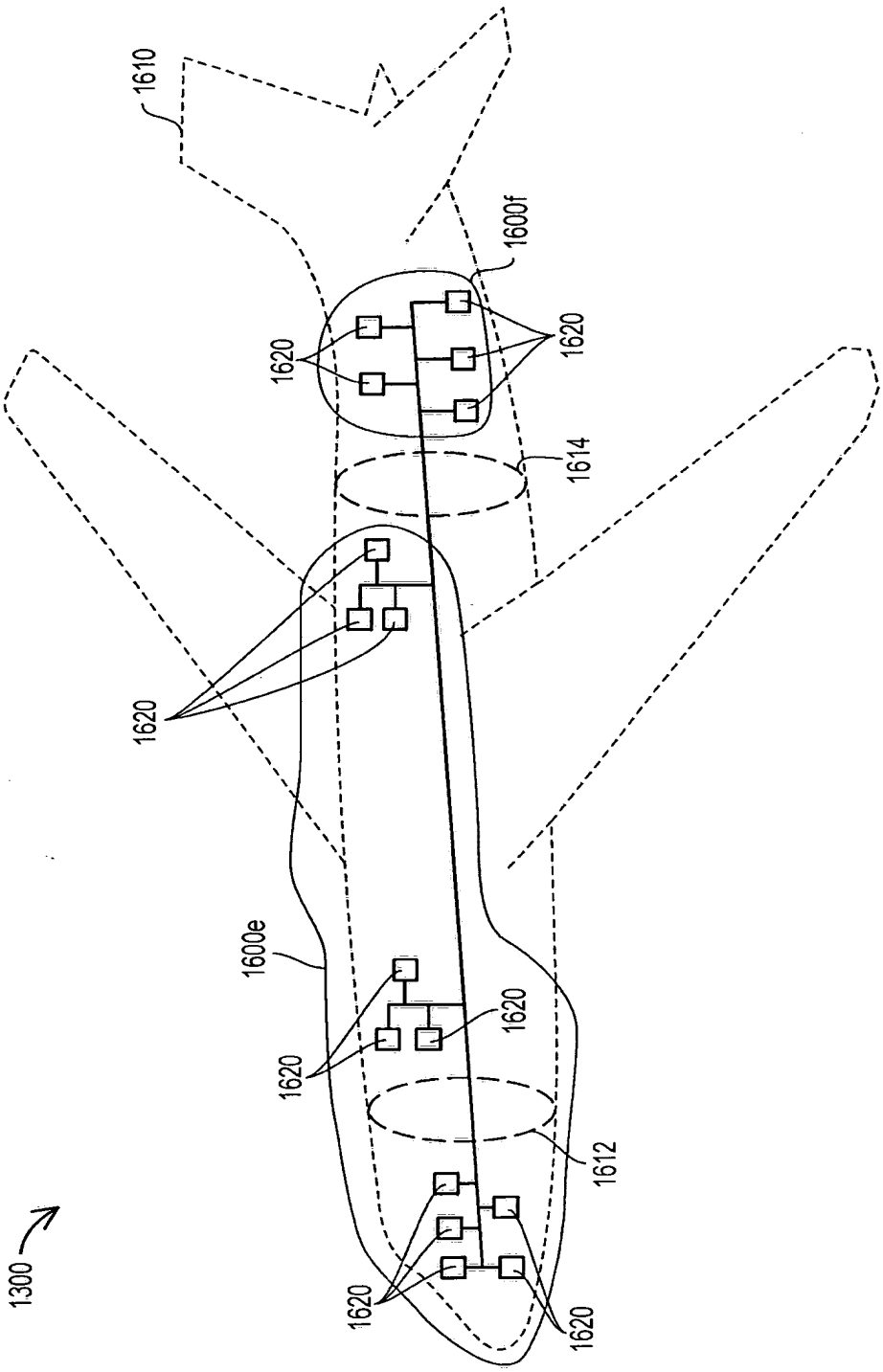

1610
1600f
1620
1620
1614
1620
1600e
1620
1620
1612
1620
1620
1300

FIG. 17

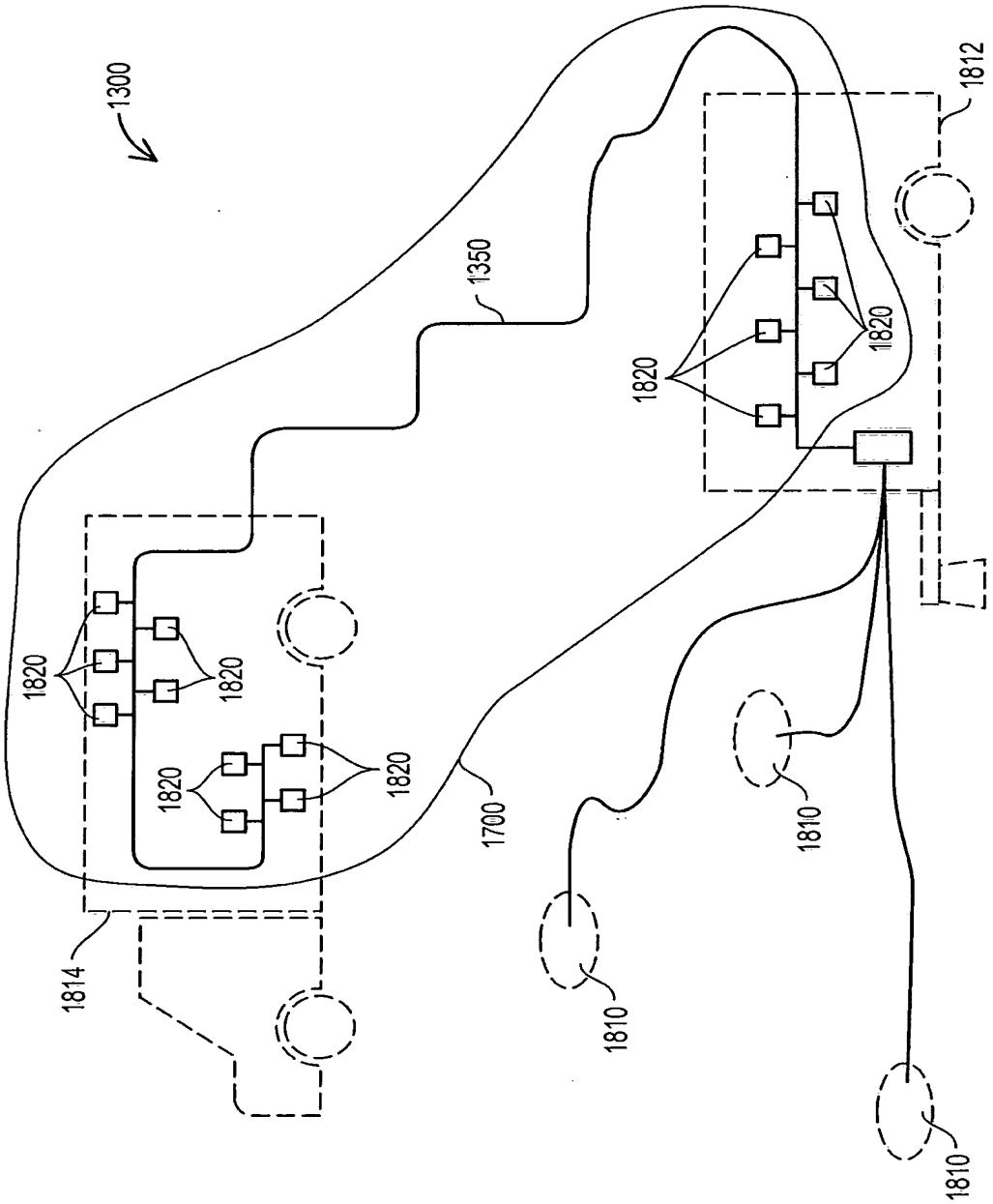

1300
1350
1812
1820
1820
1820
1820
1820
1820
1700
1810
1810
1810
1814

FIG. 18

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JERRY W. YANCEY ET AL.
Filed:	HEREWITH
For:	RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS
Serial No.:	UNKNOWN
Group Art Unit:	UNKNOWN
Examiner:	UNKNOWN
Atty Dkt:	LCOM:057

EXPRESS MAIL CERTIFICATION

NUMBER: EV978890499US

I hereby certify that this paper or fee is being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" service, postage prepaid, under 37 C.F.R. 1.10 on the date indicated below and is addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313.

Signature: Marty Jones — Date of Deposit: 11/16/06

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98, it is respectfully requested that this Information Disclosure Statement be entered and the document(s) listed on attached Form PTO-1449 be considered by the Examiner and made of record.

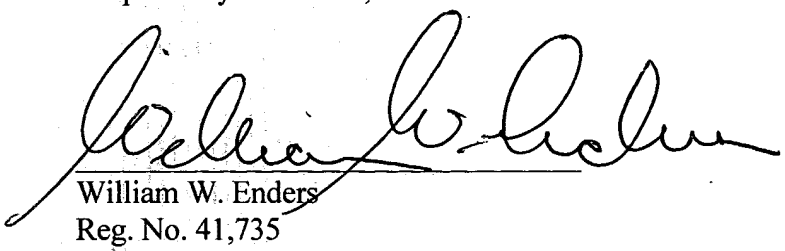
In accordance with 37 C.F.R §§ 1.97(g),(h), this Information Disclosure Statement is not to be construed as a representation that a search has been made, and is not to be construed to be an admission that (a) the information cited is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b); and/or (b) that the information cited is, or is considered to be prior art.

The present Information and Disclosure Statement is being filed prior to the receipt of a first Official Action reflecting an examination on the merits, and hence is believed to be timely filed in accordance with 37 C.F.R. § 1.97(b). No fees are believed to be due in connection with the filing of this Information Disclosure Statement, however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to these materials, the Commissioner is hereby authorized to deduct said fees from Deposit Account No. 10-1205/LCOM:057.

A copy of the listed document(s) required by 37 C.F.R. § 1.98(a)(2) is enclosed for the convenience of the Examiner.

Applicant respectfully requests that the listed document(s) be made of record in the present case.

Respectfully submitted,



William W. Enders
Reg. No. 41,735
Attorney for Applicant

O'KEEFE, EGAN & PETERMAN, LLP
1101 Capital of Texas Highway South
Building C, Suite 200
Austin, Texas 78746
(512) 347-1611
FAX: (512) 347-1615

Enclosures

Form PTO-1449 (modified)	Atty. Docket No. LCOM:057	Serial No. UNKNOWN
List of Patents and Publications for Applicant's **INFORMATION DISCLOSURE STATEMENT** (Use several sheets if necessary)	Applicant JERRY YANCEY ET AL. .	
	Filing Date: HEREWITH	Group: UNKNOWN

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Pages 1-3*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A1	6,617,877	9/9/03	Cory et al.			3/1/02
	A2	6,651,225	11/18/03	Lin et al.			4/10/00
	A3	6,421,251	7/16/02	Lin			2/5/98
	A4	6,389,379	5/14/02	Lin et al.			6/12/98
	A5	US2005/0256 969A1	11/17/05	Yancey et al.			5/11/04
	A6	6,496,291	12/17/02	Raj et al.			10/17/00
	A7	US2002/0095 400A1	7/18/02	Johnson et al.			6/12/01
	A8	US2002/0059 274A1	5/16/02	Hartsell et al.			6/12/01
	A9	6,901,072	5/31/05	Wong			5/15/03

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C1	Laxdal, "ELEC 563 Project Reconfigurable Computers", http://www.ece.uvic.ca/~elaxdal/Elec563/reconfigurable_computers.html; printed from the Internet December 19, 2003, December 2, 1999, 10 pgs.
	C2	"PCI/DSP-4 Four Complete Channels Of Digital Acoustic Emission Data Acquisition On A Single Board", http://www.pacndt.com/products/Multichannel/pcidsp.html, printed from the Internet December 19, 2003, 3 pgs.

Examiner:	**Date Considered:**

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449 (modified)	Atty. Docket No. LCOM:057	Serial No. UNKNOWN
List of Patents and Publications for Applicant's	Applicant JERRY YANCEY ET AL. .	
INFORMATION DISCLOSURE STATEMENT	Filing Date: HEREWITH	Group: UNKNOWN
(Use several sheets if necessary)		

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Pages 1-3*

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C3	Zaiq Technologies, "Innovation: Methodology Briefs", http://www.zaiqtech.com/innovation/m_fpga.html, printed from the Internet January 15, 2004, 12 pgs.
	C4	Hardt et al, "Flysig: Dataflow Oriented Delay-Insensitive Processor For Rapid Prototyping Of Signal Processing", (obtained from Internet December, 2003), 6 pgs.
	C5	Chang et al., "Evaluation Of Large Matrix Operations On A Reconfigurable Computing Platform For High Performance Scientific Computations," (obtained from Internet December, 2003), 10 pgs.
	C6	Alfke, "FPGA Configuration Guidelines," XAPP, 090 November 24, 1997, Version 1.1, pps. 31-38.
	C7	"XC18V00 Series Of In-System Programmable Configuration PROMs", Xilinx Product Specification, DS026 (v.3.0), November 12, 2001, 19 pgs.
	C8	Thacker, "System ACE Technology: Configuration Manager Breakthrough", New Technology, FPGA Configuration, Xcell Journal, Summer 2001, pps. 52-55.
	C9	"System ACE MPM Solution", Xilinx Product Specification, DS087 (v1.0) September 25, 2001, 29 pgs.
	C10	"RapidIO™: An Embedded System Component Network Architecture", Architecture And Systems Platforms, February 22, 2000, 25 pgs.
	C11	"Raceway Internlink Functional Specification", Mercury Computer Systems, Inc., November 8, 2000, 118 pgs.
	C12	"[XMC-3310] High Speed Transceiver ePMC Module", Spectrum Signal Processing, http://www.spectrumsignal.com/Products/_Datasheets/XMC-3310_datasheet.asp, (©2002-2004), 5 pgs. (this reference describes a product available prior to the May 11, 2004 filing date of the present application)
	C13	"XMC-3310 High Speed Transceiver ePMC Module", Spectrum Signal Processing, Rev. May, 2004, 4 pgs. (this reference describes a product available prior to the May 11, 2004 filing date of the present application)
	C14	RocketIO™ Transceiver User Guide, Xilinx, UG024 (v2.3) February 24, 2004, 152 pgs.
	C15	"The FPGA Systems Connectivity Tool", Product Brief, Nallatech, DIMEtalk 2.1, February 2004, pps 1-8.

Examiner:	**Date Considered:**

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449 (modified)	Atty. Docket No. LCOM:057	Serial No. UNKNOWN
List of Patents and Publications for Applicant's **INFORMATION DISCLOSURE STATEMENT** (Use several sheets if necessary)	Applicant JERRY YANCEY ET AL. .	
	Filing Date: HEREWITH	Group: UNKNOWN

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Pages 1-3*

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C16	B. Hall, "BTeV Front End Readout & Links", BTEV Co., August 17, 2000, 11 pgs.
	C17	Irwin, "Usage Models For Multi-Gigabit Serial Transceivers", Xilinx, xilinix.com, White Paper, WP157 (v1.0), March 15, 2002, 10 pgs.
	C18	Campenhout, "Computing Structures And Optical Interconnect: Friends Or Foes?", Department of Electronics And Information Systems, Ghent University, Obtained from Internet October 8, 2006, 11 pgs.
	C19	E. Hazen, "HCAL HO Trigger Link", Optical SLB-HTR Interface Specification, May 24, 2006, 4 pgs.
	C20	G. Russell, "Analysis And Modelling Of Optically Interconnected Computing Systems", School of Engineering And Physical Sciences, Heriot-Watt University, May 2004, 170 pgs.
	C21	Copending Patent Application Serial No. 11/529,712; LCOM:011C1, entitled "Systems And Methods For Interconnection Of Multiple FPGA Devices", filed September 28, 2006; 42 pgs.
	C22	Copending Patent Application Serial No. 11/529,713; LCOM:011C2, entitled "Systems And Methods For Interconnection Of Multiple FPGA Devices", filed September 28, 2006; 42 pgs.

Examiner:	**Date Considered:**

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JERRY W. YANCEY ET AL.
Filed:	HEREWITH
For:	RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS
Serial No.:	UNKNOWN
Group Art Unit:	UNKNOWN
Examiner:	UNKNOWN
Atty Docket No.:	LCOM:057

EXPRESS MAIL CERTIFICATION

NUMBER: EV978890499US

I hereby certify that this paper or fee is being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" service, postage prepaid, under 37 C.F.R. 1.10 on the date indicated below and is addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313.

Signature: Mary Jones

Date of Deposit: 11/16/06

MAIL STOP PATENT APPLICATION
Commissioner For Patents
P. O. Box 1450
Alexandria, VA 22313

Dear Sir:

Transmitted herewith for filing are:

☒ New Continuation-In-Part Patent Application consisting of 54 pages and 18 pages of Figs.

☐ Continued Prosecution Application (37 CFR §1.53(d)) -- The parent application is USSN _____ filed on _____. The prior Examiner was _____ in Group Art Unit _____.

☐ Response to Missing Parts

☐ Assignment and Recordation Cover sheet

☐ Inventors' Declaration/Power of Attorney

☐ Request and Certification Under 35 U.S.C. 122(b)(2)(B)(i)

☒ Information Disclosure Statement, PTO Form 1449; A1-A9; C1-C22

☐ Petition for a _____ month extension of time

☐ Response to Office Action

☐ Preliminary Amendment

☐ Formal Drawings

☐ Informal Drawings

☐ Notice of Appeal

☐ An Appeal Brief (an original and two copies)

☐ Check in the amount of $

☐ The Commissioner is authorized to deduct any requisite fees under 37 CFR 1.16 to 1.21 from, or deposit any credits to, Deposit Account No. 10-1205/ , including any concurrent or future required extension of time fees.

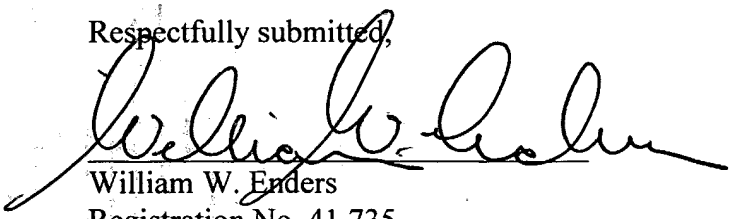
☒ In accordance with 37 CFR 1.136(a)(3), the Commissioner is authorized to treat any concurrent or future reply that requires a petition for an extension of time under 37 CFR 1.126(a) to be timely, as incorporating a petition for extension of time for the appropriate length of time, and the Commissioner is authorized to deduct any requisite extension of time fees under 37 CFR 1.16 to 1.21 from Deposit Account No. 10-1205.

☒ Postcard. Please date stamp and mail this postcard to acknowledge receipt of the enclosed documents.

☐ Other:

The Examiner is invited to contact the undersigned at 512-347-1611 with any questions or comments, or to otherwise facilitate expeditious prosecution of the application.

Respectfully submitted,



William W. Enders
Registration No. 41,735
Attorney for Applicant

O'KEEFE, EGAN & PETERMAN, L.L.P.
1101 Capital of Texas Highway South
Building C, Suite 200
Austin, Texas 78746
512-347-1611
512-347-1615 (Fax)

PTO/SB/06 (12-04)
Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD
Substitute for Form PTO-875

11/600,934

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)		OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))							300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))							500
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))							200
TOTAL CLAIMS (37 CFR 1.16(i))	34 minus 20=	14	X$25=		OR	X$50	700
INDEPENDENT CLAIMS (37 CFR 1.16(h))	4 minus 3 =	1	X$100=			X$200=	200
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			N/A			N/A	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1900

APPLICATION AS AMENDED – PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)		OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X =		OR	X =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X =		OR	X =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(					N/A		OR	N/A	
					TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)		OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X =		OR	X =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X =		OR	X =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(					N/A		OR	N/A	
					TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to comp including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comr on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. I and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JERRY W. YANCEY ET AL.
Filed:	NOVEMBER 16, 2006
For:	RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS
Serial No.:	11/600,934
Group Art Unit:	UNKNOWN
Examiner:	UNKNOWN
Atty Dkt:	LCOM:057

Pursuant to 37 C.F.R. 1.8, I certify that this correspondence is being deposited with the U.S. Postal Service in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313

Date 11/28/06 Name

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the document(s) listed on attached Form PTO-1449 be considered by the Examiner and made of record.

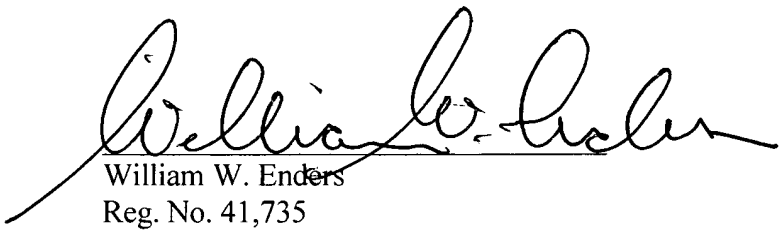
In accordance with 37 C.F.R §§ 1.97(g),(h), this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made, and is not to be construed to be an admission that (a) the information cited is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b); and/or (b) that the information cited is, or is considered to be prior art.

The present Supplemental Information and Disclosure Statement is being filed prior to the receipt of a first Official Action reflecting an examination on the merits, and hence is believed to be timely filed in accordance with 37 C.F.R. § 1.97(b). No fees are believed to be due in connection with the filing of this Supplemental Information Disclosure Statement, however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to these materials, the Commissioner is hereby authorized to deduct said fees from Deposit Account No. 10-1205/LCOM:057.

A copy of the listed document(s) required by 37 C.F.R. § 1.98(a)(2) is enclosed for the convenience of the Examiner.

Applicant respectfully requests that the listed document(s) be made of record in the present case.

Respectfully submitted,



William W. Enders
Reg. No. 41,735
Attorney for Applicant

O'KEEFE, EGAN & PETERMAN, LLP
1101 Capital of Texas Highway South
Building C, Suite 200
Austin, Texas 78746
(512) 347-1611
FAX: (512) 347-1615

Enclosures

Form PTO-1449 (modified)

List of Patents and Publications for Applicant's

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty. Docket No. LCOM:057	Serial No. 11/600,934
Applicant JERRY YANCEY ET AL. .	
Filing Date: 11/16/06	Group: UNKNOWN

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page	*See Page*	*See Page 1*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A1						

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C23	Copending Patent Application Serial No. 11/600,935; LCOM:056, entitled "Methods And Systems For Relaying Data Packets", filed November 16, 2006; 101 pgs.

Examiner:	Date Considered:

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
11/600,934	11/16/2006	2133	0.00	LCOM:057	18	34	4

CONFIRMATION NO. 4821

O'KEEFE, EGAN & PETERMAN, L.L.P.
Building C, Suite 200
1101 Capital of Texas Highway
Austin, TX78746

FILING RECEIPT

Date Mailed: 12/08/2006

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please mail to the Commissioner for Patents P.O. Box 1450 Alexandria Va 22313-1450. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Jerry W. Yancey, Residence Not Provided;
Yea Zong Kuo, Residence Not Provided;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CIP of 10/843,226 05/11/2004

Foreign Applications

If Required, Foreign Filing License Granted: 12/07/2006

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US11/600,934**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

Reconfigurable communications infrastructure for ASIC networks

Preliminary Class

714

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of

Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
11/600,934	11/16/2006	Jerry W. Yancey	LCOM:057

CONFIRMATION NO. 4821

FORMALITIES LETTER

O'KEEFE, EGAN & PETERMAN, L.L.P.
Building C, Suite 200
1101 Capital of Texas Highway
Austin, TX 78746

Date Mailed: 12/08/2006

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
  Applicant must submit $ **300** *to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).*
- The oath or declaration is missing. *A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.*
  Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Additional claim fees of **$900** as a non-small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.
- To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$2030** for a non-small entity

- **$300** Statutory basic filing fee.
- **$130** Surcharge.

- The application search fee has not been paid. Applicant must submit **$500** to complete the search fee.
- The application examination fee has not been paid. Applicant must submit **$200** to complete the examination fee for a non-small entity.

- Total additional claim fee(s) for this application is **$900**

  - **$200** for **1** independent claims over 3.
  - **$700** for **14** total claims over 20.

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
11/600,934	11/16/2006	Jerry W. Yancey	LCOM:057

CONFIRMATION NO. 4821

O'KEEFE, EGAN & PETERMAN, L.L.P.
Building C, Suite 200
1101 Capital of Texas Highway
Austin, TX 78746

FORMALITIES LETTER

Date Mailed: 12/08/2006

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
  Applicant must submit $ **300** *to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).*
- The oath or declaration is missing. *A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.*
  Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Additional claim fees of **$900** as a non-small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.
- To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of $130 for a non-small entity, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **$2030** for a non-small entity

12/28/2006 MBELETE1 00000018 11600934

01 FC:1011		300.00 OP
02 FC:1051		130.00 OP
03 FC:1111		500.00 OP
04 FC:1311		200.00 OP
05 FC:1201		200.00 OP
06 FC:1202		700.00 OP

- **$300** Statutory basic filing fee.
- **$130** Surcharge.

- The application search fee has not been paid. Applicant must submit **$500** to complete the search fee.
- The application examination fee has not been paid. Applicant must submit **$200** to complete the examination fee for a non-small entity.

- Total additional claim fee(s) for this application is **$900**

  - **$200** for **1** independent claims over 3.
  - **$700** for **14** total claims over 20.

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JERRY W. YANCEY ET AL.
Filed:	NOVEMBER 16, 2006
For:	RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS
Serial No.:	11/600,934
Group Art Unit:	2133
Examiner:	UNKNOWN
Atty Docket No.:	LCOM:057

Pursuant to 37 C.F.R. 1.8, I certify that this correspondence is being deposited with the U.S. Postal Service in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313 on the date below:

12/21/06 Marty Jones
Date Name

MAIL STOP MISSING PARTS
Commissioner For Patents
P. O. Box 1450
Alexandria, VA 22313

Dear Sir:

Transmitted herewith for filing are:

☐ New Patent Application consisting of __ pages

☐ Continued Prosecution Application (37 CFR §1.53(d)) -- The parent application is USSN _____ filed on _____. The prior Examiner was _____ in Group Art Unit _____.

☒ Notice to File Missing Parts - Part 2 copy

☐ Assignment and Recordation Cover sheet

☒ Inventors' Declaration

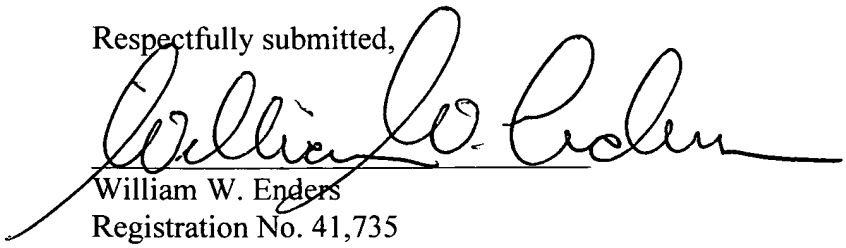
☐ Information Disclosure Statement

☐ Petition for a _____ month extension of time

- ☐ Response to Office Action
- ☐ Preliminary Amendment
- ☐ Formal Drawings (Figs , sheets)
- ☐ Informal Drawings
- ☐ Notice of Appeal
- ☐ An Appeal Brief (an original and two copies)
- ☒ Check in the amount of $2,030.00
- ☒ The Commissioner is authorized to deduct any requisite fees under 37 CFR 1.16 to 1.21 from, or deposit any credits to, Deposit Account No. 10-1205/LCOM:057, including any concurrent or future required extension of time fees.
- ☒ In accordance with 37 CFR 1.136(a)(3), the Commissioner is authorized to treat any concurrent or future reply that requires a petition for an extension of time under 37 CFR 1.136(a) to be timely, as incorporating a petition for extension of time for the appropriate length of time, and the Commissioner is authorized to deduct any requisite extension of time fees under 37 CFR 1.16 to 1.21 from Deposit Account No. 10-1205.
- ☒ Postcard. Please date stamp and mail this postcard to acknowledge receipt of the enclosed documents.
- ☒ Other: Statement Under 37 CFR 3.73(b), Election Under 37 CFR 3.71 and Power of Attorney with copy of assignment

The Examiner is invited to contact the undersigned at 512-347-1611 with any questions or comments, or to otherwise facilitate expeditious prosecution of the application.

Respectfully submitted,



William W. Enders
Registration No. 41,735
Attorney for Applicant

O'KEEFE, EGAN, PETERMAN & ENDERS, L.L.P.
1101 Capital of Texas Highway South
Building C, Suite 200
Austin, Texas 78746
512-347-1611
512-347-1615 (Fax)

DECLARATION
FOR PATENT APPLICATION

As a undersigned inventor, I hereby declare that:

My residence, post office address and country of citizenship are as stated directly below my name.

I believe (check one) [ ] I am the original, first and sole inventor
[X] I am a joint inventor and the below named inventors are the original and first inventors

of the subject matter which is claimed and for which a patent is sought on the invention entitled

RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS

the specification of which
(check one) [ ] is attached hereto.
[X] was filed on November 16, 2006,
as Application Serial No. 11/600,934,
and was amended on _____.
(if applicable)

I further declare that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office (hereinafter "the Office") all information known to me to be material to patentability of the subject matter which is claimed as defined in 37 C.F.R. §1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119 of any foreign application(s) for patent or inventor's certificate indicated below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s) Number	Country	Day/Month/Year Filed	Priority Claimed Yes	No
_____	_____	_____	___	X

I hereby claim the benefit under 35 U.S. C. §119(e) of any United States provisional application listed below:

Provisional Application Serial No. **Filing Date**

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose to the Office all information known to me to be material to patentability as defined in 37 C.F.R. § 1.56, which became available between the filing date of the prior application and the national or PCT international filing date of this application:

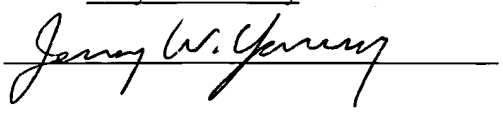
Application Serial No.	**Filing Date**	**Status (patented, pending, abandoned)**
10/843,226	5/11/04	Pending

Address all correspondence and telephone calls to the following:

William W. Enders
O'KEEFE, EGAN, PETERMAN & ENDERS
1101 Capital of Texas Highway South
Building C, Suite 200
Austin, TX 78746
(512) 347-1611
(512) 347-1615 (Fax)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and may jeopardize the validity of the application or any patent issued thereon.

Full name of first inventor: Jerry W. Yancey

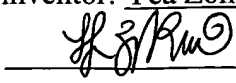
Inventor's Signature  12/13/06
Date

Residence: 5911 Sceptre Drive, Rockwall, Texas 75032

Citizenship: U.S.A.

Post Office Address: Same as above
(enter "same" if mailing address is same as residence address)

Full name of second inventor: Yea Zong Kuo

Inventor's Signature  12/14/2006
Date

Residence: 5911 Sceptre Drive, Rockwall, Texas 75032

Citizenship: U.S.A.

Post Office Address: Same as above
(enter "same" if mailing address is same as residence address)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JERRY W. YANCEY ET AL.
Filed:	NOVEMBER 16, 2006
For:	RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS
Serial No.:	11/600,934
Group Art Unit:	UNKNOWN
Examiner:	UNKNOWN
Atty Dkt:	LCOM:057

Pursuant to 37 C.F.R. 1.8, I certify that this correspondence is being deposited with the U.S. Postal Service in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date below:

12/21/06 Mary Jones

Date Name

Commissioner For Patents
P. O. Box 1450
Alexandria, VA 22313

STATEMENT UNDER 37 C.F.R. §3.73(b), ELECTION UNDER 37 C.F.R. §3.71, and POWER OF ATTORNEY

Sir:

This document provides a Statement under §3.73 by the Assignee, an Election by the Assignee under §3.71 to prosecute at the exclusion of the inventor(s), and a Power of Attorney from the Assignee.

Statement Under §3.73(b)

The undersigned states that it is the Assignee of the entire right, title and interest in the Patent application identified above by virtue of either:

A. ☒ An Assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

OR

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as shown below:

1. From: _____ To: _____ The document was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

2. From:_____ To: _____ The document was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____ The document was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet.

☒ Copies of assignments or other documents in the chain of title are attached.

[NOTE: A separate copy *(i.e.,* the original assignment document or a true copy of the original document) must be submitted to Assignment Division in accordance with 37 CFR Part 3, if the assignment is to be recorded in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is empowered to sign this statement on behalf of the assignee.

Election under §3.71

The Assignee hereby elects under 37 C.F.R. §3.71 to prosecute the application to the exclusion of the inventor(s).

Power of Attorney

The Assignee revokes any previous Powers of Attorney and appoints Robert M. O'Keefe, Reg. No. 35,630; Richard D. Egan, Reg. No. 36,788; Brian W. Peterman, Reg. No. 37,908, and William W. Enders, Reg. No. 41,735, each an attorney of the firm of O'KEEFE, EGAN & PETERMAN, LLP, as its attorney for so long as they remain with such firm with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the Patent and Trademark Office in connection therewith, and to receive any Letters Patent, and for one year after issuance of such Letters Patent to file any request for a certificate of correction that may be deemed appropriate.

Future Communications

Please direct all communications as follows:

William W. Enders
O'KEEFE, EGAN , PETERMAN & ENDERS, LLP
1101 Capital of Texas Highway South
Building C, Suite 200
Austin, Texas 78746
512/347-1611
FAX 512/347-1615

ASSIGNEE:

L-3 Integrated Systems Company

By: _____
(Signature)

Name: Steven M. Post

Date: 12/15/2006

Title: General Counsel and Vice President, Contracts

FILE NO. LCOM:057
PATENT

ASSIGNMENT

FOR GOOD AND VALUABLE CONSIDERATION, the receipt, sufficiency and adequacy of which are hereby acknowledged, the undersigned, do hereby:

SELL, ASSIGN AND TRANSFER to L-3 INTEGRATED SYSTEMS COMPANY (the "Assignee"), being incorporated under the laws of the State of Delaware, having a place of business 10001 Jack Finney Blvd., Greenville, Texas 75402, the entire right, title and interest for the United States and all foreign countries in and to (1) any and all improvements which are disclosed in the application for United States Letters Patent, Serial No. 11/600,934, filed on November 16, 2006 and is entitled "RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS" (2) such application and all divisional, continuing, continuation-in-part, substitute, renewal, reissue and all other applications for patent which have been or shall be filed in the United States and all foreign countries on any of such improvements; and (3) any and all original and reissued patents which have been or shall be issued in the United States and all foreign countries on such improvements; and specifically including the right to file foreign applications under the provisions of any convention or treaty and claim priority based on such applications in the United States;

AUTHORIZE AND REQUEST the issuing authority to issue any and all United States and foreign patents granted on such improvements to the Assignee;

WARRANT AND COVENANT that no assignment, grant, mortgage, license or other agreement affecting the rights and property herein conveyed has been or will be made to others by the undersigned, and that the full right to convey the same as herein expressed is possessed by the undersigned;

COVENANT, when requested and at the expense of the Assignee, to carry out in good faith the intent and purpose of this assignment, the undersigned will execute all divisional, continuing, substitute, renewal, reissue, and all other patent applications on any and all such improvements; execute all rightful oaths, declarations, assignments, powers of attorney and other papers; communicate to the Assignee all facts known to the undersigned relating to such improvements and the history thereof; and generally do everything possible which the Assignee shall consider desirable for vesting title to such improvements in the Assignee, and for securing, maintaining and enforcing proper patent protection for such improvements;

TO BE BINDING on the heirs, assigns, representatives and successors of the undersigned and extend to the successors, assigns and nominees of the Assignee.

(Signature): Jerry W. Yancey Date: 12/13/06

Jerry W. Yancey

State of Texas)
County of Hunt)

BEFORE ME, the undersigned authority, on this 13th day of December, 2006 personally appeared Jerry W. Yancey, known to me to be the person whose name is subscribed to the foregoing instrument and acknowledged to me that he executed the same of his own free will for the purposes and consideration therein expressed.

[SEAL] CAROL S. LANGFORD MY COMMISSION EXPIRES July 9, 2009

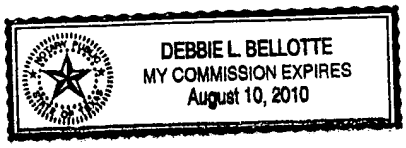
Carol S. Langford
Notary or Consular Officer

Signature): _____ Date: 12/14/2006
Yea Zong Kuo

State of Texas)
County of Rockwall)

BEFORE ME, the undersigned authority, on this 14 day of December, 2006 personally appeared Yea Zong Kuo, known to me to be the person whose name is subscribed to the foregoing instrument and acknowledged to me that he executed the same of his own free will for the purposes and consideration therein expressed.

[SEAL]



_____
Notary or Consular Officer

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
11/600,934	11/16/2006	2133	2030	LCOM:057	18	34	4

CONFIRMATION NO. 4821

O'KEEFE, EGAN & PETERMAN, L.L.P.
Building C, Suite 200
1101 Capital of Texas Highway
Austin, TX78746

UPDATED FILING RECEIPT

Date Mailed: 01/10/2007

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please mail to the Commissioner for Patents P.O. Box 1450 Alexandria Va 22313-1450. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Jerry W. Yancey, Rockwall, TX;
Yea Zong Kuo, Rockwall, TX;

Power of Attorney:
Robert O'Keefe--35630
Richard Egan--36788
Brian Peterman--37908
William Enders--41735

Domestic Priority data as claimed by applicant

This application is a CIP of 10/843,226 05/11/2004

Foreign Applications

If Required, Foreign Filing License Granted: 12/07/2006

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US11/600,934**

Projected Publication Date: 04/19/2007

Non-Publication Request: No

Early Publication Request: No

Title

Preliminary Class

714

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/600,934	11/16/2006	Jerry W. Yancey	LCOM:057

CONFIRMATION NO. 4821

36275
O'KEEFE, EGAN, PETERMAN & ENDERS LLP
1101 CAPITAL OF TEXAS HIGHWAY SOUTH
#C200
AUSTIN, TX78746

Title: Reconfigurable communications infrastructure for ASIC networks

Publication No. US-2007-0101242-A1
Publication Date: 05/03/2007

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 703-305-3028.

Pre-Grant Publication Division, 703-605-4283

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	PATENT NUMBER	GROUP ART UNIT	FILE WRAPPER LOCATION
11/600,934		2112	

Correspondence Address / Fee Address Change

The following fields have been set to Customer Number 36275 on 03/01/2007

- Correspondence Address

The address of record for Customer Number 36275 is:
O'KEEFE, EGAN, PETERMAN & ENDERS LLP
1101 CAPITAL OF TEXAS HIGHWAY SOUTH
#C200
AUSTIN,TX 78746

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JERRY W. YANCEY ET AL.
Filed:	NOVEMBER 16, 2006
For:	RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS
Serial No.:	11/600,934
Group Art Unit:	2133
Examiner:	UNKNOWN
Atty Dkt:	LCOM:057

Pursuant to 37 C.F.R. 1.8, I certify that this correspondence is being deposited with the U.S. Postal Service in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313

6/5/07 — Date

Name

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the document(s) listed on attached Form PTO-1449 be considered by the Examiner and made of record.

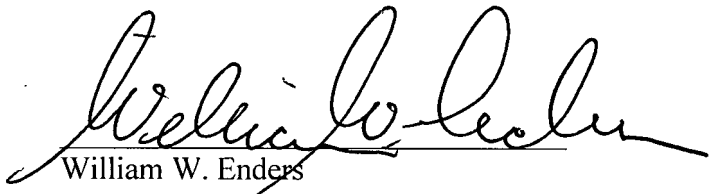
In accordance with 37 C.F.R §§ 1.97(g),(h), this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made, and is not to be construed to be an admission that (a) the information cited is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b); and/or (b) that the information cited is, or is considered to be prior art.

The present Supplemental Information and Disclosure Statement is being filed prior to the receipt of a first Official Action reflecting an examination on the merits, and hence is believed to be timely filed in accordance with 37 C.F.R. § 1.97(b). No fees are believed to be due in connection with the filing of this Supplemental Information Disclosure Statement, however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to these materials, the Commissioner is hereby authorized to deduct said fees from Deposit Account No. 10-1205/LCOM:057.

A copy of the listed document(s) required by 37 C.F.R. § 1.98(a)(2) is enclosed for the convenience of the Examiner.

Applicant respectfully requests that the listed document(s) be made of record in the present case.

Respectfully submitted,



William W. Enders
Reg. No. 41,735
Attorney for Applicant

O'KEEFE, EGAN, PETERMAN & ENDERS, LLP
1101 Capital of Texas Highway South
Building C, Suite 200
Austin, Texas 78746
(512) 347-1611
FAX: (512) 347-1615

Enclosures

Form PTO-1449 (modified)

List of Patents and Publications for Applicant's

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty. Docket No.	Serial No.
LCOM:057	11/600,934
Applicant: JERRY YANCEY ET AL. .	
Filing Date: 11/16/06	Group: 2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Pages 1-2	*See Page*	*See Page*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A10	7,035,228	4/25/06	Baumer			10/29/03
	A11	US2005/0183 042A1	8/18/05	Vogel et al.			12/2/03
	A12	6,721,313	4/13/04	Van Duyne			8/1/00
	A13	6,259,693	7/10/01	Ganmukhi et al.			8/28/97
	A14	US2004/0249 964A1	12/9/04	Mougel			3/6/03
	A15	US2004/0085 902A1	5/6/04	Miller et al.			3/5/03
	A16	6,172,927	1/9/01	Taylor			3/24/00
	A17	6,965,571	11/15/05	Webber			8/27/01
	A18	7,188,283	3/6/07	Shafer et al.			9/11/03
	A19	6,292,923	9/18/01	Genrich et al.			3/24/00
	A20	US2004/0131 072A1	7/8/04	Khan et al.			8/12/03
	A21	6,873,180	3/29/05	Bentz			3/24/03
	A22	5,941,988	8/24/99	Bhagwat et al.			1/27/97
	A23	6,496,505	12/17/02	La Porta et al.			12/11/98
	A24	6,934,763	8/23/05	Kubota et al.			3/21/01
	A25	US2002/0021 680A1	2/21/02	Chen			7/30/01
	A26	US2002/0057 657A1	5/16/02	La Porta et al.			12/11/98
	A27	US2003/0009 585A1	1/9/03	Antoine et al.			12/17/01
	A28	US2005/0175 018A1	8/11/05	Wong			11/29/04

Examiner: | **Date Considered:**

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449 (modified)	Atty. Docket No. LCOM:057	Serial No. 11/600,934
List of Patents and Publications for Applicant's **INFORMATION DISCLOSURE STATEMENT** (Use several sheets if necessary)	Applicant JERRY YANCEY ET AL. .	
	Filing Date: 11/16/06	Group: 2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Pages 1-2	*See Page*	*See Page*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A29	US2006/0002386A1	1/5/06	Yik et al.			6/30/04

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation

Examiner:	**Date Considered:**

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

IFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JERRY W. YANCEY ET AL.
Filed:	NOVEMBER 16, 2006
For:	RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS
Serial No.:	11/600,934
Group Art Unit:	2133
Examiner:	UNKNOWN
Atty Dkt:	LCOM:057

Pursuant to 37 C.F.R. 1.8, I certify that this correspondence is being deposited with the U.S. Postal Service in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313

8/1/07 — Date

Mary Goins — Name

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the document(s) listed on attached Form PTO-1449 be considered by the Examiner and made of record.

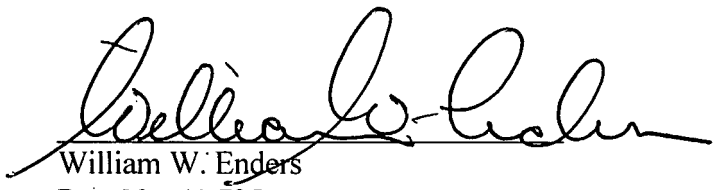
In accordance with 37 C.F.R §§ 1.97(g),(h), this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made, and is not to be construed to be an admission that (a) the information cited is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b); and/or (b) that the information cited is, or is considered to be prior art.

The present Supplemental Information and Disclosure Statement is being filed prior to the receipt of a first Official Action reflecting an examination on the merits, and hence is believed to be timely filed in accordance with 37 C.F.R. § 1.97(b). No fees are believed to be due in connection with the filing of this Supplemental Information Disclosure Statement, however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to these materials, the Commissioner is hereby authorized to deduct said fees from Deposit Account No. 10-1205/LCOM:057.

A copy of the listed document(s) required by 37 C.F.R. § 1.98(a)(2) is enclosed for the convenience of the Examiner.

Applicant respectfully requests that the listed document(s) be made of record in the present case.

Respectfully submitted,



William W. Enders
Reg. No. 41,735
Attorney for Applicant

O'KEEFE, EGAN, PETERMAN & ENDERS, LLP
1101 Capital of Texas Highway South
Building C, Suite 200
Austin, Texas 78746
(512) 347-1611
FAX: (512) 347-1615

Enclosures

Form PTO-1449 (modified)

List of Patents and Publications for Applicant's

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty. Docket No.	Serial No.
LCOM:057	11/600,934
Applicant: JERRY YANCEY ET AL.	
Filing Date: 11/16/06	Group: 2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Page*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A30	6,381,238	4/30/02	Hluchyj			7/31/98
	A31	US2005/0248364A1	11/10/05	Vadi et al.			4/30/04
	A32	6,333,641	12/25/01	Wasson			5/5/00
	A33	US2005/0044439A1	2/24/05	Shatas et al.			9/10/04
	A34	6,888,376	5/3/05	Venkata et al.			9/24/03

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation

Examiner: | **Date Considered:**

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

JFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JERRY W. YANCEY ET AL.
Filed:	NOVEMBER 16, 2006
For:	RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS
Serial No.:	11/600,934
Group Art Unit:	2133
Examiner:	UNKNOWN
Atty Dkt:	LCOM:057

Pursuant to 37 C.F.R. 1.8, I certify that this correspondence is being deposited with the U.S. Postal Service in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313

11/13/07 — Date

Name

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the document(s) listed on attached Form PTO-1449 be considered by the Examiner and made of record.

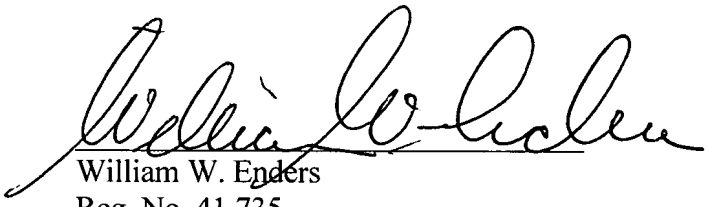
In accordance with 37 C.F.R §§ 1.97(g),(h), this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made, and is not to be construed to be an admission that (a) the information cited is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b); and/or (b) that the information cited is, or is considered to be prior art.

The present Supplemental Information and Disclosure Statement is being filed prior to the receipt of a first Official Action reflecting an examination on the merits, and hence is believed to be timely filed in accordance with 37 C.F.R. § 1.97(b). No fees are believed to be due in connection with the filing of this Supplemental Information Disclosure Statement, however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to these materials, the Commissioner is hereby authorized to deduct said fees from Deposit Account No. 10-1205/LCOM:057.

A copy of the listed document(s) required by 37 C.F.R. § 1.98(a)(2) is enclosed for the convenience of the Examiner.

Applicant respectfully requests that the listed document(s) be made of record in the present case.

Respectfully submitted,



William W. Enders
Reg. No. 41,735
Attorney for Applicant

O'KEEFE, EGAN, PETERMAN & ENDERS, LLP
1101 Capital of Texas Highway South
Building C, Suite 200
Austin, Texas 78746
(512) 347-1611
FAX: (512) 347-1615

Enclosures

Form PTO-1449 (modified)

List of Patents and Publications for Applicant's

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty. Docket No.	Serial No.
LCOM:057	11/600,934
Applicant	
JERRY YANCEY ET AL.	
Filing Date:	**Group:**
11/16/06	2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Page*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A35	US2005/0169311A1	8/4/05	Millet et al.			1/29/04
	A36	7,137,048	11/14/06	Zerbe et al.			10/12/01
	A37	6,201,829	3/13/01	Schneider			4/3/98
	A38	6,385,236	5/7/02	Chen			10/5/98
	A39	5,953,372	9/14/99	Virzi			12/13/96
	A40	US2004/0158784A1	8/12/04	Abuhamdeh et al.			8/22/03
	A41	7,003,585	2/21/06	Phong et al.			9/5/01
	A42	6,020,755	2/1/00	Andrews et al.			9/26/97

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation

Examiner: | **Date Considered:**

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JERRY W. YANCEY ET AL.
Filed:	NOVEMBER 16, 2006
For:	RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS
Serial No.:	11/600,934
Group Art Unit:	2133
Examiner:	UNKNOWN
Atty Dkt:	LCOM:057

Pursuant to 37 C.F.R. 1.8, I certify that this correspondence is being deposited with the U.S. Postal Service in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313

11/20/07 — Date

J. McArthur — Name

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the document(s) listed on attached Form PTO-1449 be considered by the Examiner and made of record.

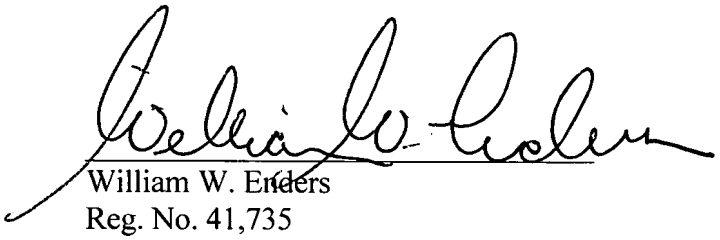
In accordance with 37 C.F.R §§ 1.97(g),(h), this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made, and is not to be construed to be an admission that (a) the information cited is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b); and/or (b) that the information cited is, or is considered to be prior art.

The present Supplemental Information and Disclosure Statement is being filed prior to the receipt of a first Official Action reflecting an examination on the merits, and hence is believed to be timely filed in accordance with 37 C.F.R. § 1.97(b). No fees are believed to be due in connection with the filing of this Supplemental Information Disclosure Statement, however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to these materials, the Commissioner is hereby authorized to deduct said fees from Deposit Account No. 10-1205/LCOM:057.

A copy of the listed document(s) required by 37 C.F.R. § 1.98(a)(2) is enclosed for the convenience of the Examiner.

Applicant respectfully requests that the listed document(s) be made of record in the present case.

Respectfully submitted,



William W. Enders
Reg. No. 41,735
Attorney for Applicant

O'KEEFE, EGAN, PETERMAN & ENDERS, LLP
1101 Capital of Texas Highway South
Building C, Suite 200
Austin, Texas 78746
(512) 347-1611
FAX: (512) 347-1615

Enclosures

Form PTO-1449 (modified)

List of Patents and Publications for Applicant's

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty. Docket No.	Serial No.
LCOM:057	11/600,934
Applicant: JERRY YANCEY ET AL.	
Filing Date: 11/16/06	Group: 2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page 1*	*See Page*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A43	6,233,704	5/15/01	Scott et al.			3/13/96

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1	GB2377138A	12/31/02	United Kingdom			Yes

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation

Examiner:	Date Considered:

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

B1

(12) UK Patent Application (19) GB (11) 2 377 138 (13) A

(43) Date of A Publication 31.12.2002

(21) Application No 0115835.1

(22) Date of Filing 28.06.2001

(71) Applicant(s)
Telefonaktiebolaget L M Ericsson
(Incorporated in Sweden)
SE-126 25, Stockholm, Sweden

(72) Inventor(s)
Rowan Nigel Naylor

(74) Agent and/or Address for Service
Haseltine Lake & Co
Imperial House, 15-19 Kingsway,
LONDON, WC2B 6UD, United Kingdom

(51) INT CL[7]
G06F 13/40 , H04L 12/42

(52) UK CL (Edition T)
H4P PPBC

(56) Documents Cited
GB 2188216 A
JP 100228445 A
US 4884192 A
EP 1069509 A2
US 4982400 A
US 4641276 A

(58) Field of Search
UK CL (Edition T) G4A AFGDC, H4P PPBC
INT CL[7] G06F 13/37 13/40, H04L 12/42 12/427 12/43 12/433
Other: Online: EPODOC, JAPIO, WPI

(54) Abstract Title
Ring Bus Structure For System On Chip Integrated Circuits

(57) A bus structure for an integrated circuit designed to accommodate the types of operation used in telecommunications systems and to reduce the required bus frequency for a given system whilst also reducing power and processing power. The bus comprises a plurality of interface modules which are connected in series to form the bus structure, where each module is operable to transfer data to at least one adjacent module in the series, and including an interface unit for connection with a host peripheral, and a storage element for storing data.

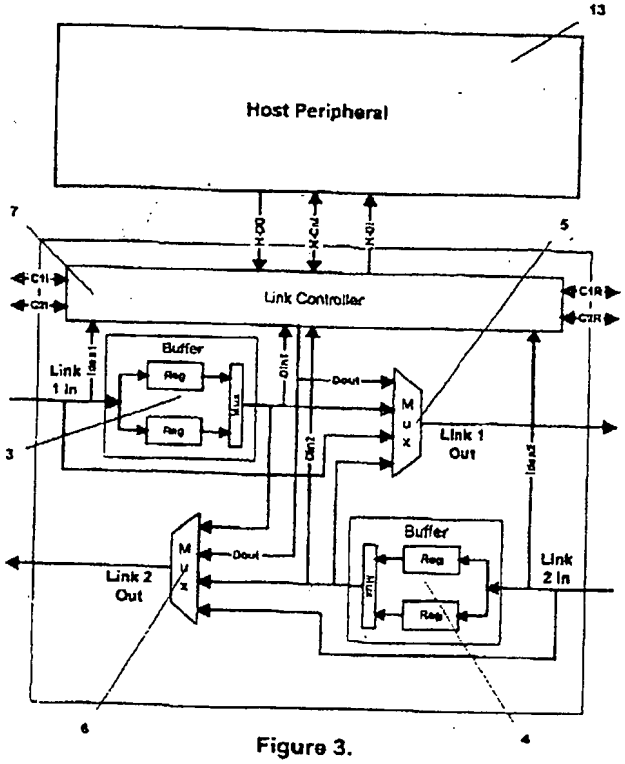


Figure 3.

GB 2 377 138 A

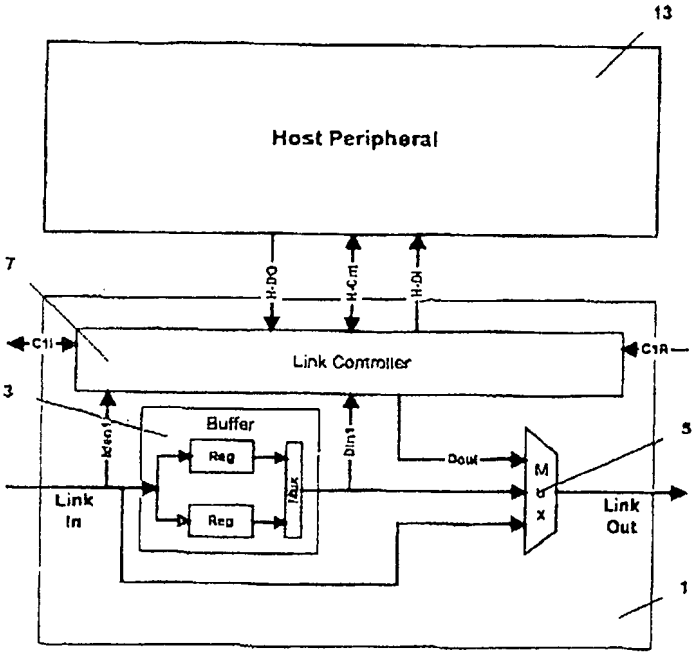


Figure 1.

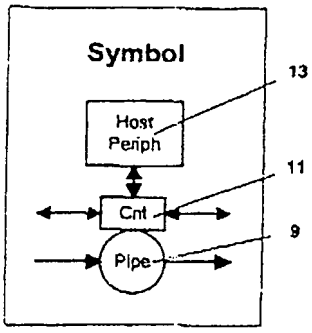


Figure 2.

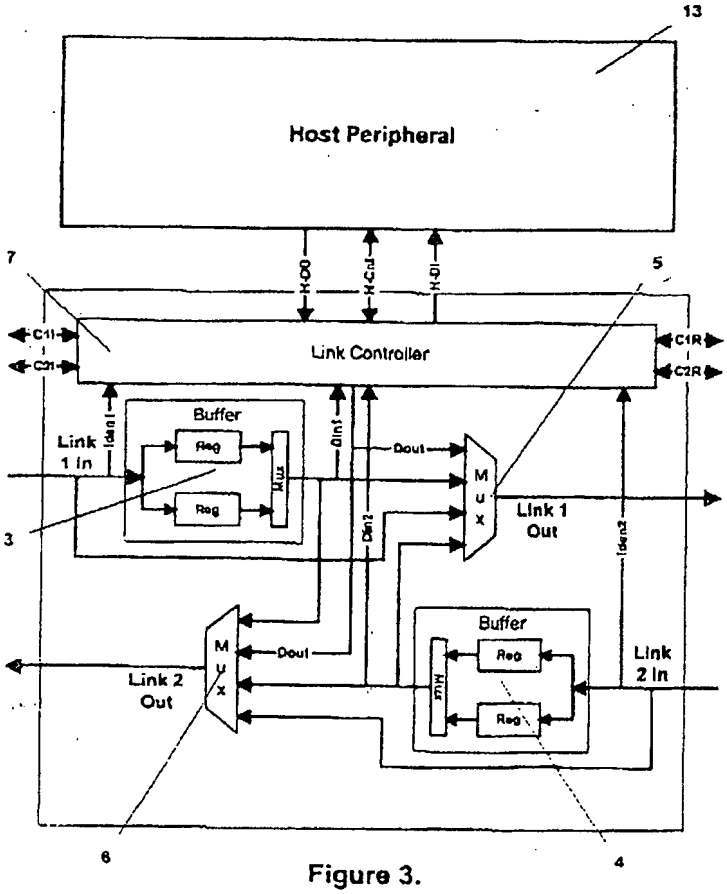


Figure 3.

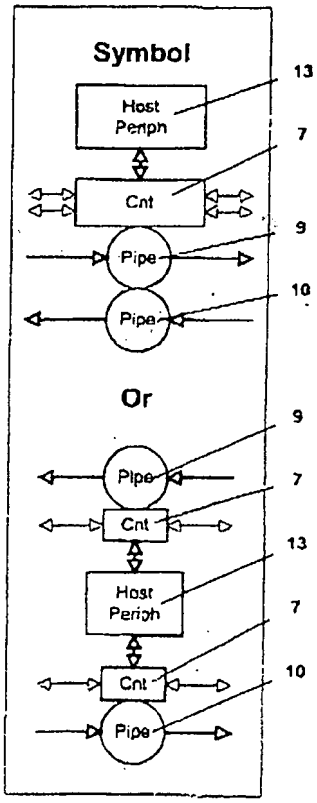
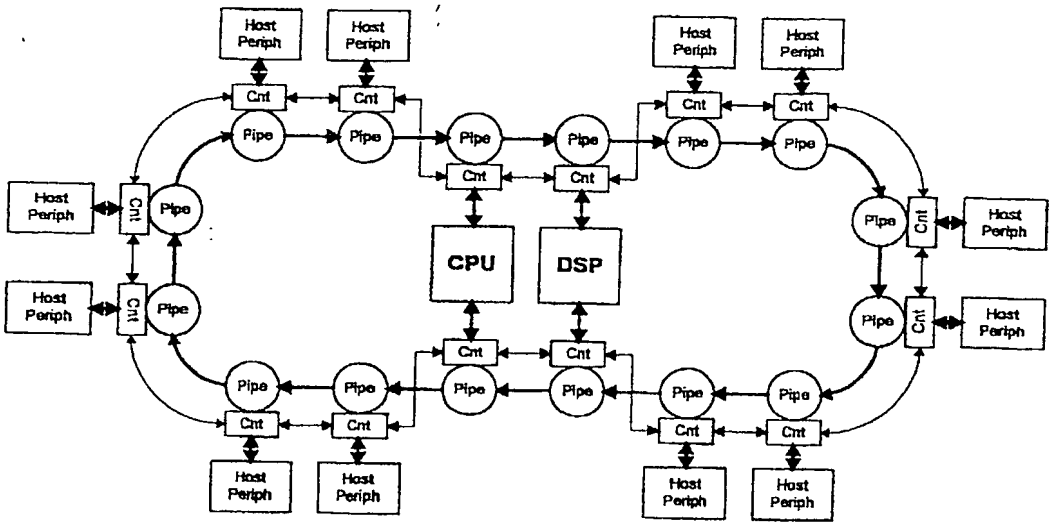
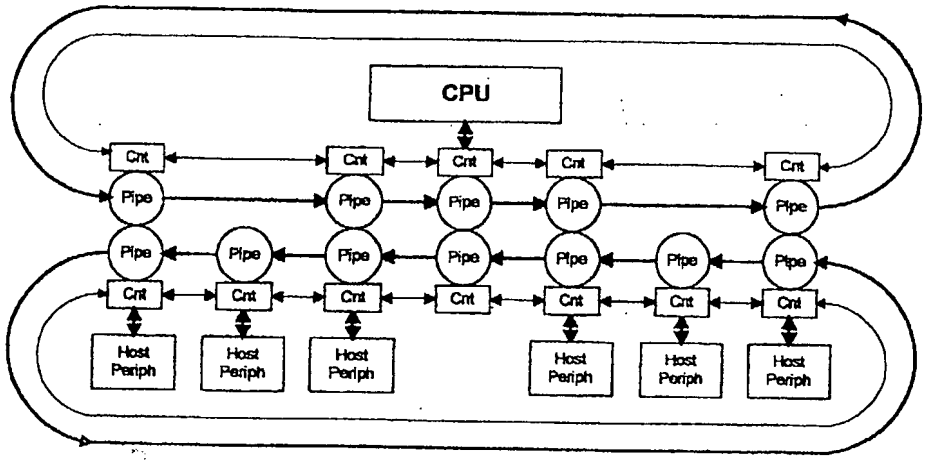


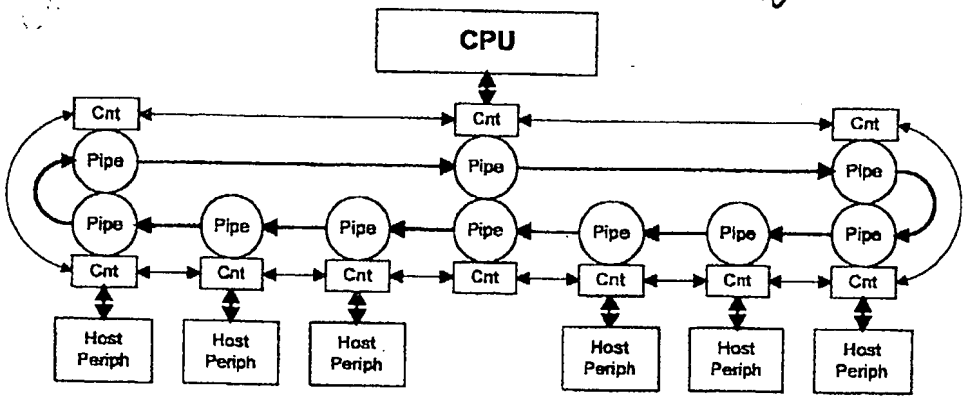
Figure 4.



Dual Processor Single Pipe Ring Example Figure 5



Dual Port - Dual Ring Bus Architecture Figure 6



Chain Ring Bus Architecture Figure 7

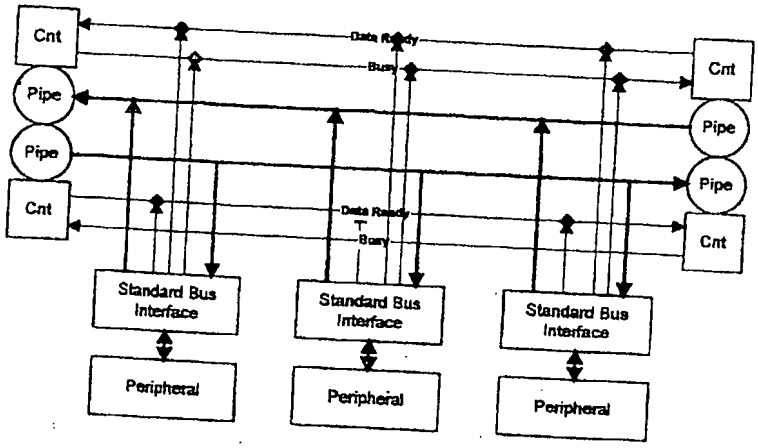

Cnt
Pipe
Pipe
Cnt
Data Ready
Busy
Data Ready
Busy
Cnt
Pipe
Pipe
Cnt
Standard Bus Interface
Standard Bus Interface
Standard Bus Interface
Peripheral
Peripheral
Peripheral

Figure 8

2377138

BUS ARCHITECTURES

The present invention relates to bus architectures for use in integrated circuits.

Background of the invention

The majority of modern 'System on Chip' (SoC) designs use known bus architectures and methodologies to implement processor driven systems. These are typically based on a master slave approach with a master unit (eg. a processor) controlling all operations on the bus and accessing slave units using memory mapped addressing. An address space is viewed as a sequential set of memory locations in which each slave unit (eg. peripheral) is assigned a collection of addresses.

The master unit controls all transfers between slave units by reading from one slave unit into a buffer and then writing to another slave unit from that buffer. This requires a two stage transfer process.

This process is simplified in some known systems by using a 'Direct Memory Access' (DMA) unit that executes this operation as back to back memory accesses. This is more efficient than using the processor itself as it can be hardwired and does not require software. However, the bus must be a multi-master design to allow control of the bus to be passed between processor and DMA unit.

In either case the maximum transfer rate of data is half the maximum rate sustainable by the bus, because there are two transfer actions required per data transfer.

In the telecommunications industry the design of a system architecture typically uses sequential sets of processes to implement a function, such as a modem. Data is passed along a series of processes in sequence,

each process modifying the data and passing it on to the next process in the series.

This can be implemented without a bus structure as such by hardwiring one hardware process block to the next. However, increasingly some of these processes are being implemented in software for processing by a DSP or CPU. In addition, in order to increase the flexibility and testability of the system it is necessary for the DSP/CPU to have access to the input and output of all process blocks in the sequence.

In the traditional bus architecture this requires each block to be memory mapped to the DSP/CPU bus, the DSP/CPU is then responsible for the passing of data between the blocks. This can be supported by a DMA unit, that is programmed by the DSP/CPU, as described above.

As the required performance of the system increases, the effect on the system bus is magnified, and so the required bandwidth reaches the limits of the technology.

For example, consider a modem implementation consisting of 5 sequential process blocks, if each block has the same data input rate and data output rate of X bytes/second then the minimum total data rate required is 10 X bytes/second.

As the data throughput of the modem increases the required bus performance has to increase by a factor of 10 which can be difficult to achieve.

In addition, the movement of data by the processor consumes substantial processing power and electrical power, both of which are at a premium ideally and need to be minimised, particularly in mobile and handheld systems.

Summary of the present invention

The bus architecture of the present invention is designed to accommodate the types of operation used in telecommunication systems and to reduce the required bus frequency for a given system while also reducing power and processing power.

It is emphasised that the term "comprises" or "comprising" is used in this specification to specify the presence of stated features, integers, steps or components, but does not preclude the addition of one or more further features, integers, steps or components, or groups thereof.

Brief description of the drawings

Figures 1 and 2 illustrate a single port bus module embodying one aspect of the present invention;

Figures 3 and 4 illustrate a dual port bus module embodying another aspect of the present invention.

Figures 5, 6 and 7 illustrate respective example bus architectures embodying the modules of Figure 1 to 4; and

Figure 8 illustrates a module of Figures 1 to 4 interfacing with a known bus interface.

Detailed description of the preferred embodiments

A single port module 1 embodying one aspect of the present invention is shown in schematic form in Figure 1 and comprises a buffer memory element 3 and a multiplexer 5, both of which are controlled by a link controller 7. The module is illustrated connected with a host peripheral 2. The link controller 7 communicates with the host peripheral 2. Figure 2 shows a symbol representation of the module of Figure 1, the buffer 3 and multiplexer 5 are represented by a pipe 9 and the link controller by unit 11. As in

Figure 1, the module 1 of Figure 1, the module 1 of Figure 2 is shown connected with a host peripheral unit 2. Data is received by the module 1 in packetised form. A data consists of one or more words, each word containing one or more data bits. Incoming data packets are presented to the link controller 7, to the buffer 3 and to the multiplexer 5. The link controller 7 examines the incoming data packets to determine what action is needed. Each data packet contains a header portion identifying the packet, and a data payload which contains the data to be transferred.

The data packet header is examined by the link controller in order to determine the action required.

Incoming data packets are always loaded into the buffer 3 when the buffer 3 is free. The multiplexer 5 is connected to receive the output from the buffer 3, data from host peripheral 2 (via the link controller 7) and the data input to the module 1. The data output from the buffer 3, can also be routed via the link controller 7 to the host peripheral 13.

The link controller 7 determines if a data packet is intended for the host 2 and routes the data packet to it if that is the case. The link controller 7 also controls the multiplexer 5 and depending on the identity of the data packet will output the data packet from the module. Modules are connected together to form a bus structure, as will be described in more detail below. If the host 2 needs to output data packets to the bus then the link controller 7 causes the multiplexer 5 to output the host data packet to the next module in the bus. The data packet can be a priority transfer so that the link controller 7 routes the data input directly to the data output of the module.

The single port module shown in Figures 1 and 2 is a uni-directional device. A bi-directional dual port

module is illustrated in Figures 3 and 4, and contains two single port modules as described above. The directions of data in the bus for each port are generally opposite to one another. In addition a link is provided from the output of the buffer 3 in one module to the multiplexer in the other module. This allows a data packet from one path of the bus to the other path.

The link controller 7 interfaces to adjacent modules in the bus structure. The link controller 7 controls handshaking signals that transfers data packets from one module to the next. In the dual ring configuration using the dual port module the two rings preferably operate independently of one another. The transfer between modules can be either asynchronous or synchronous as required by the system design; the basic operation is the same.

Data packets are transferred along the bus from module to module.

The bus architecture can take the form of a ring when the last link in a chain of links is attached to the first in the chain; this allows data to be transferred between all links in the chain.

In the dual port link architecture a ring can be formed in a chain by linking the two ports of both the first and last link in the chain or a dual ring and 'mobius' ring by joining the last and first links in the chain.

Figures 5, 6 and 7 illustrate example bus architectures using the modules of Figures 1 to 4.

At any given time, the maximum data rate on the bus will be equal to the speed of the slowest link multiplied by the number of buffers in the ring. For example if there are 10 links in the ring, each with one word of buffering, and a transfer rate of 1M

packets per second, then the maximum bus data rate is 10M packets/second.

Each module presents the same single load to the previous module in the series forming the bus structure. Therefore as modules are added to the bus the overall loading on most of the existing modules is unaffected. Also, the speed of the bus is determined by the aggregate loading of the modules, which can be faster than in known bus architectures because of the lower loading on a given module.

The transfer of data packets between any two modules depends on the number of other modules between them. This is a latency that needs to be taken into account when setting up the bus structure. Given that this bus architecture is designed to service object/message based communication the latency can be considered to affect only the first word of a transfer; all subsequent words arrive at the destination at full speed since they would have the same latency. As a result the effective data rate is the total time, (latency time plus data transfer time) divided by the number of transfers. The larger the data packets transferred the lower the aggregate effect of the latency.

As described above, transfer of data packets between modules is controlled by the Link Controller 7 (LC) of each module. The link controller 7 is responsible for controlling the transfer of data packets into the buffer 3 and the subsequent use of the output multiplexer. The LC 7 also controls the transfer of data packets to and from the host peripheral using the link interface.

The transfer control is also basically the same for both asynchronous and synchronous operation, the only difference being that in the synchronous case all actions take place with respect to a clock edge, and in

the asynchronous case they take place as quickly as possible.

A two-signal handshake is used for the transfer and moves one data packet from one module to the next module.

An overall data transfer may contain multiple data packets that are sent sequentially. In such a case the same transfer mechanism operates as for single data packet transfers except the header structure is modified. The first packet of the transfer contains a full header and all subsequent data packets contain only the link identifier with the last word containing an indicator showing end of package.

The link controller at a destination for the payload ensures that the package is reconstructed. Also the sequence of transfers are treated as continuous in that no host peripheral between source and destination is allowed to insert a package midway through the sequence.

If the receiving link is busy, either the next link ahead to it is busy or the host is inserting a payload then the transmitting link is held off for as long as required.

The buffer 3 of the link interface may be capable of storing more than data packet, using a FIFO structure. This can be used to reduce the delays incurred in inserting data packets.

In a ring structure there exists the possibility of a lock-up in which a delay forces the busy signal to be active in all modules, that is the delay in a module accepting data ripples back around the ring till it is itself halted by a busy signal ahead.

This can occur if all modules already contain payloads filling their buffers 3 but not directed at them and then another payload is inserted by a host.

This is prevented by giving the contents of the buffer 3 priority over data to be inserted by the host. The host can only insert data if its buffer 3 is not full.

This is tempered with the ability to 'Force' data onto the bus by temporarily removing the contents of the full buffer 3 associated with the link doing the forcing.

This mechanism allows a host with priority payload to accept the payload aimed at another link and substitute its own. The intercepted payload can then be either discarded or sent when capacity is available.

The host peripheral attached to the intercepting interface makes the choice based on how much local memory is available. In the case of limited local memory then the data would be discarded. The receiving peripheral using the header information would detect the missing data and request retransmission of the lost data.

However, the method uses the buffer in the interface and then signals controlling the transfer are caused to ripple back to the transmitting peripheral to halt its data transfer.

The mechanism works by double buffering incoming data on a halt. The interface that is inserting data does not pass on the present data stored in the buffer but instead accepts the next data packet into a second buffer register while indicating to the previous interface that it is busy.

The previous interface stops transfer of the new data in its buffer but accepts data from its previous interface into its second register while indicating it is busy. This is repeated back along the chain to the source peripheral that stops transmission of reception of a busy signal.

When the inserting interface releases its interface, data is output from the first register in its buffer followed by the data in the second register as normal and retaining the order of the data. On the output of the second register data it signals to the previous interface that it is no longer busy and accepts data from the interface.

The previous interface responds to its previous interface in the same fashion, and this control signal ripples back to the source which restarts sending data.

In normal operation only one of the two registers in the buffer are used, the other is dormant.

The header of the data packet includes information relating to a host identifier to indicate the module, an object identifier to indicate the type and name of the data packet and possibly a further object identifier indicating to which of a number of similar objects the data packet belongs.

The bus architecture embodying the present invention uses such identifiers to allow a data packet to be treated as a distinct object that may be applicable to one or more host peripherals. This feature allows a system using these identifiers to be scaled up and down without affecting the bus design. Software using this method can be re-used without knowing the topology of the hardware on which it is working.

Preferably, a flag is associated with the header to determine which of two types it is, a destination or source identifier header. The header type controls how the data packet is treated by the link controller 7.

If the header is a destination type, then the link identifier in the header is used to select the destination host peripheral for the data packet via its associated bus module. When the data packet reaches

its destination, the data is read and is not transferred to the next link.

If the identifier is a source type the link identifier indicates from which host peripheral the payload is being sent or broadcast. If a host peripheral accepts the source and object identifiers in the header as relevant to it, the data packet will be copied and sent onto the next module in the series.

This also provides a mechanism which allows the host peripheral generating the data packet (the source) to confirm transmission of the data packet around the bus. This is accomplished when the source receives a data packet with its own source identifier in the header.

This method also allows a data packet to be sent to multiple host peripherals without having to use multiple data packets as is common in the known bus architectures.

Providing both link and object identifiers in the data packet header allows selectivity based on the type of data and not just on an explicit address. It allows data to be grouped for selective processing. An example of its use in a telecommunications application would be the processing of audio data.

In such a scheme, data from an input source can be routed to multiple host peripherals: a DSP for coding and transmission, a voice recognition module for a command interface, and a memory store if a memo function is required, for example.

In addition such a scheme supports sequential processing of data through a chain of operations contained in the host peripherals.

For example:

Consider an input data packet given a source identifier that relates to a frame in a sequence of

frames and an object identifier that indicates the stage of processing.

Such a data packet would be accepted by a host based on its object identifier, the data would be processed and a new data packet generated with the same source identifier but a new object identifier indicating the processing stage to which the data packet has reached.

This is repeated through the series of host peripherals until it reaches the end of the processing sequence. The last stage uses the source identifier is used to ensure the processed frames remain in order. At any point in the sequence if the process cannot be completed then an error data packet can be generated for transmission to the last processing stage to allow it to resolve the error.

Such a bus structure must ideally be able to be used with legacy peripherals which are based on a standard processor bus architecture. Such a scheme is illustrated in Figure 8. Legacy peripherals can make use of a bus structure embodying the present invention by being placed between two dual port modules. The bus inputs to the peripheral are mounted on one bus and the outputs on the other. In operation they are treated as above using the 'By-Pass' link of the module. Data from one module is input to all standard peripherals. If the identifier is recognised, then it is treated as a simple address, and the interface acknowledges it and blocks the data available signal to the following module thereby preventing acceptance of the data.

If a peripheral addressed in this manner needs to output data then it also forces the busy signal active to the same module to prevent it outputting data on the other bus. It then outputs its data to interface A and indicates the presence of data. The data is maintained

until interface A accepts it, at which point the controlled signals are released.

Some advantages of embodiments of the present invention are presented below:

The standard bus architecture data rate varies between a maximum of the highest speed peripheral and a minimum determined by the slowest peripheral, with a maximum determined by the physical technology of the implementation. In systems with lots of peripherals this results in multiple buses which increases complexity and hence risk and cost.

In contrast, a bus architecture embodying the present invention provides a maximum data rate as a function of the sum total of all data rates of the peripherals. Each link between adjacent modules is limited to a maximum data rate determined by the physical technology but the overall data rate for the bus is not, which leads to a data rate greater than that of a known bus. Also, the physical placement and architecture of embodiments of the present invention should lead to lower complexity and easier testing which reduces risk. Additionally, in embodiments of the present invention, all interfaces to the host peripherals are the same further reducing complexity and testing overheads.

In standard bus architectures the sum loading of all peripherals on the bus limits the maximum speed achievable for a given technology. The higher the load, the higher the drive current required and therefore the higher the power consumed.

In embodiments of the present invention, each module in the bus represents a single load to the previous module. This can be much less than the loading experienced in a standard bus architecture. The number of host peripherals on the bus does not therefore limit the speed of operation due to loading.

Adding more modules to the bus will affect the latency but not the speed of operation.

In standard bus architectures only one peripheral can access another at any given time. As a result the data rate required of a standard bus for a given system is the sum of the total data rates required by each peripheral.

Embodiments of the present invention support multiple parallel communication between host peripherals on different parts of the bus. By placing the peripherals to make use of this the maximum data rate of the system is effectively increased and hence the lifetime of the technology is extended which itself can reduce design costs.

In standard bus architectures when a master unit drives the bus all peripherals are driven; only one address responds but all interfaces have to determine if they are the destination. This results in wasted power consumption for those interfaces which are not addressed.

In embodiments of the present invention, only the host peripherals involved in the communication and the intervening host peripherals are active during data packet transfer, all others are idle and take no part in the transfer. If the bypass link in a module is used in intervening interfaces the activity is further reduced. This can reduce bus activity and therefore power consumption, especially if a self-timed technique is used for implementation.

Software written for standard bus architectures uses absolute addressing and explicit use of the memory locations to identify parameters/objects in the host peripheral. In a new system employing the same peripherals the address may be altered required changes to the software. This requires time for both changes and verification that is costly in most new projects.

Software written for a system using a bus architecture embodying the present invention can be re-used in other systems containing the same host peripherals without modification. This is because the use of object based identifiers in the data packet headers allow parameters and data objects in peripherals to be used without knowing their physical location. This reduces software modifications, and hence cost, and increases re-usability.

In order to reduce latency of a bus architecture embodying the present invention, the modules interfaces between the two modules that require fast access are by-passed the maximum delay being the sum of these small delays. The placement of peripherals can minimise the number of intervening modules such that in such a high-speed mode the latency is equivalent to the standard bus architecture.

Systems using standard buses with two or more processors generally do not allow the driving of peripherals by more than one processor. If a second processor needs to access a peripheral this is achieved by request to the first processor. This reduces the available processing capacity of the first processor for its normal operation, requires specific code on the first processor, and can lead to access conflicts. Such an arrangement can also have a high non-deterministic latency. All of these factors increase the risk, development time and cost of a system.

In contrast, multi-processor systems using embodiments of the present invention allow local use of peripherals associated with a processor but also allow direct access to those peripherals by other processors. No special code is required, and no specific communication between processors is required, since it can be co-ordinated by the shared peripheral. In

addition, latency is more deterministic (and in fact shorter). These factors can reduce risk and cost.

Known system architectures using known buses implement complex data transfer mechanisms when applied to modern telecommunications and related applications. The data flow at the abstract level does not always fit the available data flow at the physical level. This results in wasted resources that limit the performance of the system and hence its lifetime in future applications, thereby increasing cost and development time.

An architecture embodying the present invention supports object and data block based processing which allows easier sequential processing while allowing maximum access to the sequence. This allows more efficient data transfer and flexibility in re-sequencing processes. This then reduces risk in the development while allowing easier addition of future applications while extending the lifetime and scope of the physical technology. The result if lower cost and shorter time to market.

The embodiments also allow broadcast, ie. one-to-many communication.

CLAIMS

1. A bus structure for an integrated circuit, the structure comprising a plurality of interface modules which are connected in series to form the bus structure, each module being operable to transfer data to at least one adjacent module in the series, and including an interface unit for connection with a host peripheral, and a storage element for storing data.

2. A structure as clamed in claim 1, wherein the storage element is operable to store data received from an adjacent module in the series.

3. A structure as claimed in claim 1 or 2, wherein the storage element is operable to store data received from the interface unit.

4. A structure as claimed in claim 1, 2 or 3, wherein the storage element is operable to output data to an adjacent module in the series.

5. A structure as claimed in claim 1, 2 or 3, wherein each module includes a multiplexer which is operable to output data received from one of the interface controller and the storage element.

6. A bus structure as claimed in any one of the preceding claims wherein data transfer between one pair of adjacent modules is independent of data transfer between another pair of adjacent modules.

7. A bus structure as claimed in any one of the preceding claims, wherein each module has an identification value.

8. A bus structure as claimed in any one of the preceding claims, wherein data is transferred along the bus structure in discrete data packets.

9. A bus structure as claimed in any one of the preceding claims, wherein the plurality of interface modules are substantially identical.

10. A bus structure comprising a series of modules, each module comprising:

an input storage element operable to receive data from an adjacent module in the series;

a module controller operable to control data transfer through the module and to exchange control information with an adjacent module in the series; and

an output multiplexer operable to output data to an adjacent module in the series, under the control of the module controller.

Application No: GB 0115835.1 **Examiner:** Owen Wheeler
Claims searched: 1-10 **Date of search:** 30 January 2002

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.T): G4A (AFGDC) H4P (PPBC)

Int Cl (Ed.7): G06F: 13/37, 13/40; H04L: 12/42, 12/427, 12/43, 12/433.

Other: Online: EPODOC, JAPIO, WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	GB 2188216 A	[PLESSEY] See abstract.	1,10 at least
X	EP 1069509 A2	[TEXAS INSTRUMENTS] See abstract and Figs. 3 and 4.	1,10 at least
X	JP 10-228445 A	[MITSUBISHI ELECTRIC] See abstract and figure.	1,10 at least
X	US 4982400 A	[EBERSOLE] See Figs. 1 and 2.	1,10 at least
X	US 4884192 A	[TERADA] See Figs. 1-3.	1,10 at least
X	US 4641276 A	[DUNKI-JACOBS] See abstract and figure.	1,10 at least

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

IFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JERRY W. YANCEY ET AL.
Filed:	NOVEMBER 16, 2006
For:	RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS
Serial No.:	11/600,934
Group Art Unit:	2133
Examiner:	UNKNOWN
Atty Dkt:	LCOM:057

Pursuant to 37 C.F.R. 1.8, I certify that this correspondence is being deposited with the U.S. Postal Service in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313

4/9/08 — Date

Name

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the document(s) listed on attached Form PTO-1449 be considered by the Examiner and made of record.

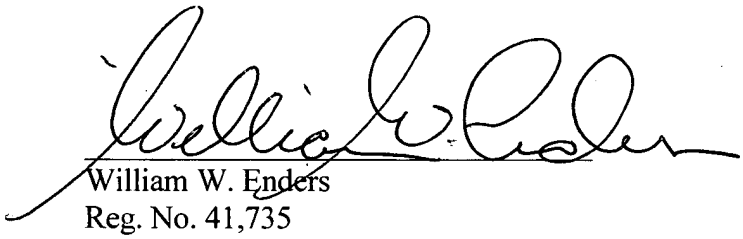
In accordance with 37 C.F.R §§ 1.97(g),(h), this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made, and is not to be construed to be an admission that (a) the information cited is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b); and/or (b) that the information cited is, or is considered to be prior art.

The present Supplemental Information and Disclosure Statement is being filed prior to the receipt of a first Official Action reflecting an examination on the merits, and hence is believed to be timely filed in accordance with 37 C.F.R. § 1.97(b). No fees are believed to be due in connection with the filing of this Supplemental Information Disclosure Statement, however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to these materials, the Commissioner is hereby authorized to deduct said fees from Deposit Account No. 10-1205/LCOM:057.

A copy of the listed document(s) required by 37 C.F.R. § 1.98(a)(2) is enclosed for the convenience of the Examiner.

Applicant respectfully requests that the listed document(s) be made of record in the present case.

Respectfully submitted,



William W. Enders
Reg. No. 41,735
Attorney for Applicant

O'KEEFE, EGAN, PETERMAN & ENDERS, LLP
1101 Capital of Texas Highway South
Building C, Suite 200
Austin, Texas 78746
(512) 347-1611
FAX: (512) 347-1615

Enclosures

Form PTO-1449 (modified)

List of Patents and Publications for Applicant's

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty. Docket No.	Serial No.
LCOM:057	11/600,934
Applicant: JERRY YANCEY ET AL.	
Filing Date: 11/16/06	Group: 2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Page*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A44	US2003/0026 260A1	2/6/03	Ogasawara et al.			8/5/02
	A45	US2004/0240 468A1	12/2/04	Chin et al.			5/30/03
	A46	US2003/0167 340A1	9/4/03	Jonsson			5/17/01
	A47	US2004/0156 368A1	8/12/04	Barri et al.			2/11/03

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation

Examiner: | **Date Considered:**

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JERRY W. YANCEY ET AL.
Filed:	NOVEMBER 16, 2006
For:	RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS
Serial No.:	11/600,934
Group Art Unit:	2133
Examiner:	UNKNOWN
Atty Dkt:	LCOM:057

Pursuant to 37 C.F.R. 1.8, I certify that this correspondence is being deposited with the U.S. Postal Service in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313

4/25/08 — Date

Name

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the document(s) listed on attached Form PTO-1449 be considered by the Examiner and made of record.

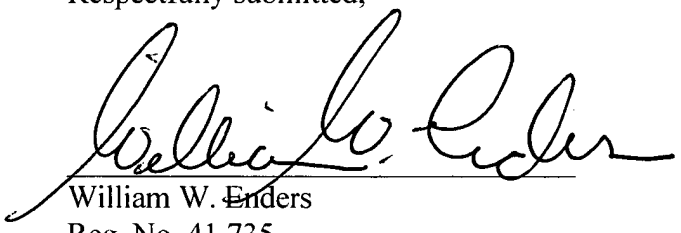
In accordance with 37 C.F.R §§ 1.97(g),(h), this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made, and is not to be construed to be an admission that (a) the information cited is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b); and/or (b) that the information cited is, or is considered to be prior art.

The present Supplemental Information and Disclosure Statement is being filed prior to the receipt of a first Official Action reflecting an examination on the merits, and hence is believed to be timely filed in accordance with 37 C.F.R. § 1.97(b). No fees are believed to be due in connection with the filing of this Supplemental Information Disclosure Statement, however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to these materials, the Commissioner is hereby authorized to deduct said fees from Deposit Account No. 10-1205/LCOM:057.

A copy of the listed document(s) required by 37 C.F.R. § 1.98(a)(2) is enclosed for the convenience of the Examiner.

Applicant respectfully requests that the listed document(s) be made of record in the present case.

Respectfully submitted,



William W. Enders
Reg. No. 41,735
Attorney for Applicant

O'KEEFE, EGAN, PETERMAN & ENDERS, LLP
1101 Capital of Texas Highway South
Building C, Suite 200
Austin, Texas 78746
(512) 347-1611
FAX: (512) 347-1615

Enclosures

Form PTO-1449 (modified)

List of Patents and Publications for Applicant's

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty. Docket No.	Serial No.
LCOM:057	11/600,934
Applicant: JERRY YANCEY ET AL.	
Filing Date: 11/16/06	Group: 2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Page 1*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A48	7,020,147	3/28/06	Amadon et al.			11/13/01
	A49	5,838,167	11/17/98	Erickson et al.			5/13/97
	A50	5,737,235	4/7/98	Kean et al.			9/6/95
	A51	US2005/0242 834A1	11/3/05	Vadi et al.			4/30/04

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C24	Search Report, PCT/US07/23700; April 18, 2008; 2 pgs.

Examiner:	Date Considered:

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JERRY W. YANCEY ET AL.
Filed:	NOVEMBER 16, 2006
For:	RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS
Serial No.:	11/600,934
Group Art Unit:	2133
Examiner:	UNKNOWN
Atty Dkt:	LCOM:057

Pursuant to 37 C.F.R. 1.8, I certify that this correspondence is being deposited with the U.S. Postal Service in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313

2-24-09 Mandy Jo
Date Name

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313

Sir:

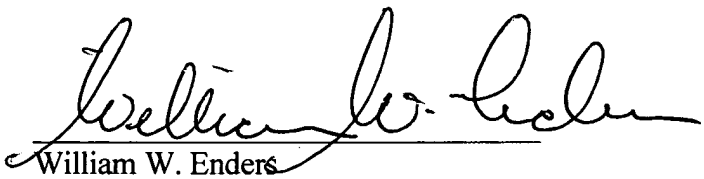
Pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the document(s) listed on attached Form PTO-1449 be considered by the Examiner and made of record.

In accordance with 37 C.F.R §§ 1.97(g),(h), this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made, and is not to be construed to be an admission that (a) the information cited is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b); and/or (b) that the information cited is, or is considered to be prior art.

The present Supplemental Information and Disclosure Statement is being filed prior to the receipt of a first Official Action reflecting an examination on the merits, and hence is believed to be timely filed in accordance with 37 C.F.R. § 1.97(b). No fees are believed to be due in connection with the filing of this Supplemental Information Disclosure Statement, however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to these materials, the Commissioner is hereby authorized to deduct said fees from Deposit Account No. 10-1205/LCOM:057.

Applicant respectfully requests that the listed document(s) be made of record in the present case.

Respectfully submitted,



William W. Enders
Reg. No. 41,735
Attorney for Applicant

O'KEEFE, EGAN, PETERMAN & ENDERS, LLP
1101 Capital of Texas Highway South
Building C, Suite 200
Austin, Texas 78746
(512) 347-1611
FAX: (512) 347-1615

Enclosures

Form PTO-1449 (modified)

List of Patents and Publications for Applicant's

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty. Docket No.	Serial No.
LCOM:057	11/600,934
Applicant: JERRY YANCEY ET AL.	
Filing Date: 11/16/06	Group: 2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Page*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A52	6,075,380	6/13/00	Lane			10/27/97
	A53	7,111,110	9/19/06	Pedersen			12/10/02
	A54	6,993,032	1/31/06	Dammann et al.			6/29/00

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation

Examiner: | **Date Considered:**

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

JPW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JERRY W. YANCEY ET AL.
Filed:	NOVEMBER 16, 2006
For:	RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS
Serial No.:	11/600,934
Group Art Unit:	2133
Examiner:	UNKNOWN
Atty Dkt:	LCOM:057

Pursuant to 37 C.F.R. 1.8, I certify that this correspondence is being deposited with the U.S. Postal Service in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313

3/3/09
Date

Name

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313

Sir:

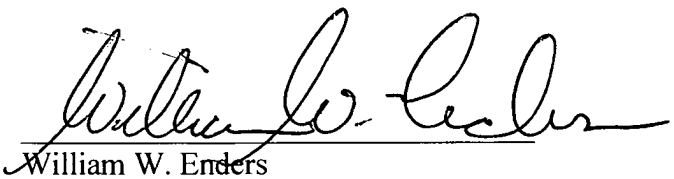
Pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the document(s) listed on attached Form PTO-1449 be considered by the Examiner and made of record.

In accordance with 37 C.F.R §§ 1.97(g),(h), this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made, and is not to be construed to be an admission that (a) the information cited is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b); and/or (b) that the information cited is, or is considered to be prior art.

The present Supplemental Information and Disclosure Statement is being filed prior to the receipt of a first Official Action reflecting an examination on the merits, and hence is believed to be timely filed in accordance with 37 C.F.R. § 1.97(b). No fees are believed to be due in connection with the filing of this Supplemental Information Disclosure Statement, however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to these materials, the Commissioner is hereby authorized to deduct said fees from Deposit Account No. 10-1205/LCOM:057.

Applicant respectfully requests that the listed document(s) be made of record in the present case.

Respectfully submitted,



William W. Enders
Reg. No. 41,735
Attorney for Applicant

O'KEEFE, EGAN, PETERMAN & ENDERS, LLP
1101 Capital of Texas Highway South
Building C, Suite 200
Austin, Texas 78746
(512) 347-1611
FAX: (512) 347-1615

Enclosures

Form PTO-1449 (modified)

List of Patents and Publications for Applicant's

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty. Docket No.	Serial No.
LCOM:057	11/600,934
Applicant: JERRY YANCEY ET AL.	
Filing Date: 11/16/06	Group: 2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Page*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A55	7,260,650	8/21/07	Lueckenhoff			11/28/01

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation

Examiner:	Date Considered:

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449 (modified)

List of Patents and Publications for Applicant's

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty. Docket No.	Serial No.
LCOM:057	11/600,934
Applicant: JERRY YANCEY ET AL.	
Filing Date: 11/16/06	Group: 2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Page*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A56	4,528,658	7/9/85	Israel			9/13/82

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation

Examiner: | **Date Considered:**

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JERRY W. YANCEY ET AL.
Filed:	NOVEMBER 16, 2006
For:	RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS
Serial No.:	11/600,934
Group Art Unit:	2133
Examiner:	UNKNOWN
Atty Dkt:	LCOM:057

Pursuant to 37 C.F.R. 1.8, I certify that this correspondence is being deposited with the U.S. Postal Service in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313

Date 6/16/09 Name

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313

Sir:

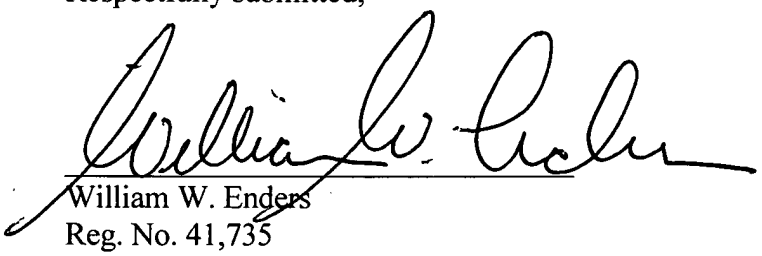
Pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the document(s) listed on attached Form PTO-1449 be considered by the Examiner and made of record.

In accordance with 37 C.F.R §§ 1.97(g),(h), this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made, and is not to be construed to be an admission that (a) the information cited is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b); and/or (b) that the information cited is, or is considered to be prior art.

The present Supplemental Information and Disclosure Statement is being filed prior to the receipt of a first Official Action reflecting an examination on the merits, and hence is believed to be timely filed in accordance with 37 C.F.R. § 1.97(b). No fees are believed to be due in connection with the filing of this Supplemental Information Disclosure Statement, however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to these materials, the Commissioner is hereby authorized to deduct said fees from Deposit Account No. 10-1205/LCOM:057.

Applicant respectfully requests that the listed document(s) be made of record in the present case.

Respectfully submitted,



William W. Enders
Reg. No. 41,735
Attorney for Applicant

O'KEEFE, EGAN, PETERMAN & ENDERS, LLP
1101 Capital of Texas Highway South
Building C, Suite 200
Austin, Texas 78746
(512) 347-1611
FAX: (512) 347-1615

Enclosures

Form PTO-1449 (modified)

List of Patents and Publications for Applicant's

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty. Docket No.	Serial No.
LCOM:057	11/600,934
Applicant: JERRY YANCEY ET AL.	
Filing Date: 11/16/06	Group: 2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Page*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A57	7,224,184	5/29/07	Levi et al.			11/5/04

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation

Examiner: | **Date Considered:**

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JERRY W. YANCEY ET AL.
Filed:	NOVEMBER 16, 2006
For:	RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS
Serial No.:	11/600,934
Group Art Unit:	2133
Examiner:	UNKNOWN
Atty Dkt:	LCOM:057

Pursuant to 37 C.F.R. 1.8, I certify that this correspondence is being deposited with the U.S. Postal Service in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313

3/4/10
Date

Name

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313

Sir:

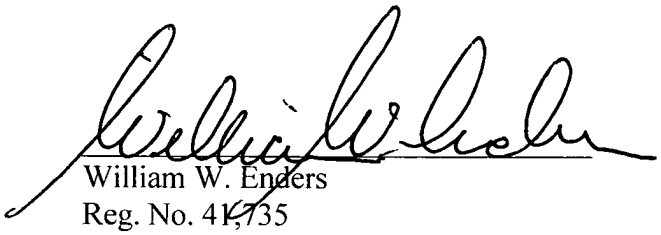
Pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the document(s) listed on attached Form PTO-1449 be considered by the Examiner and made of record.

In accordance with 37 C.F.R §§ 1.97(g),(h), this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made, and is not to be construed to be an admission that (a) the information cited is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b); and/or (b) that the information cited is, or is considered to be prior art.

The present Supplemental Information and Disclosure Statement is being filed prior to the receipt of a first Official Action reflecting an examination on the merits, and hence is believed to be timely filed in accordance with 37 C.F.R. § 1.97(b). No fees are believed to be due in connection with the filing of this Supplemental Information Disclosure Statement, however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to these materials, the Commissioner is hereby authorized to deduct said fees from Deposit Account No. 10-1205/LCOM:057.

Applicant respectfully requests that the listed document(s) be made of record in the present case.

Respectfully submitted,



William W. Enders
Reg. No. 41,735
Attorney for Applicant

O'KEEFE, EGAN, PETERMAN & ENDERS, LLP
1101 Capital of Texas Highway South
Building C, Suite 200
Austin, Texas 78746
(512) 347-1611
FAX: (512) 347-1615

Enclosures

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/600,934	11/16/2006	Jerry W. Yancey	LCOM:057	4821

36275 7590 06/23/2010

O'KEEFE, EGAN, PETERMAN & ENDERS LLP
1101 CAPITAL OF TEXAS HIGHWAY SOUTH
#C200
AUSTIN, TX 78746

EXAMINER	
BAKER, STEPHEN M	
ART UNIT	PAPER NUMBER
2112	

MAIL DATE	DELIVERY MODE
06/23/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/600,934	YANCEY ET AL.	
	Examiner	Art Unit	
	Stephen M. Baker	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 November 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *111606-030810 (12)*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

The terms “ASIC” and “FPGA” do not appear to be used consistently or in a standard way in the specification. More specifically, it is not explained how “ASIC device” are to be considered an example of “FPGA devices” as suggested in various portions of the specification ([0002], [0010}, [0013], [0015], [0016], [0018], [0019], [0055], [0073], [00891], [0090], [0100], [0106] and [0109]), or equatable to “field programmable devices (FPDs)” or "programmable logic devices (PLDs)" [0010].

Copending application data has been left blank [0099].

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1, 16, 27 and 31, the intended meaning of “ASIC devices” is unclear in view of the specification and common terminology. Reference is hereby made to the objection to the disclosure. Applicant appears to be using the term “ASIC

device" to include any device that has at least one ASIC chip and/or at least one form of programmable logic chip.

Further regarding claim 1, "providing a high bandwidth interconnection medium coupled between said packet routers of each of said two or more ASIC devices to form a reconfigurable communications infrastructure" is taken to indicate that providing an "interconnection medium" for a set of packet routers is considered to inherently form a "reconfigurable communications infrastructure" for the set of packet routers.

Regarding claims 2-15, 17-26, 29, 30, 33 and 34, equating "FPGA devices" to "ASIC devices" is considered confusing in view of standard definitions that apparently treat the two types of device names as distinct and non-overlapping. It may be that the "ASIC devices" referred to are ASIC chips supplemented with one or more field-programmable gate arrays included on-chip, however this is not clear from the disclosure alone.

Further regarding claim 3, "providing said two or more FPGA devices by providing two or more signal processing circuits" is unclear and apparently should be "configuring said two or more FPGA devices to provide two or more signal processing circuits" or the like.

Further regarding claim 4, "said packet router of each one of said two or more FPGA devices of said at least one signal processing circuit being coupled to each respective packet router of each of the other of said two or more FPGA devices of said at least one signal processing circuit" is confusing and apparently should be "said packet router of each one of said two or more FPGA devices of one of said signal

processing circuits being coupled to each respective packet router of each of the other of said two or more FPGA devices of another of said signal processing circuits" or the like, and "using said packet router of each given one of said two or more FPGA devices of one of said signal processing circuits to communicate data packets with each other of said two or more FPGA devices of another of said signal processing circuits" or the like.

Further regarding claims 5, 19 and 20, confusing language similar to claim 4 is apparent.

Further regarding claim 15, "said third computing" apparently should be "said third computing cluster."

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 7,506,297 to Mukherjee *et al* ("Mukherjee").

Mukherjee discloses an automated software tool for reconfiguring a hybrid FPGA network, the hybrid FPGA network being a network implemented with a plurality of FPGAs (column 5, lines 61-64). Mukherjee suggests (column 7, lines 2-5) that any type of network topology and connection can be handled by the automated software tool. Examples of network (12) topologies mentioned by Mukherjee include torus networks

and mesh networks (column 6, line 30) and the network topology can reconfigured (column 6, lines 31-32). The hybrid FPGA network (Fig. 2) can include a plurality of cluster nodes or grid nodes (22) each connected to an FPGA board block (24). Each node (22) is a host machine for an associated FPGA board block (24), and may be implemented with a client or server computer (column 6). Each FPGA board block includes at least one FPGA board (28). Communication between the FPGA boards and within the FPGA boards can involve any type of interconnection arrangement (column 6, lines 54-56). An FPGA board is shown (Fig. 4) comprising two FPGAs (32) and two memory chips (34), the FPGAs and memory blocks being interconnected by multi-gigabit busses (44), with each FPGA comprising one or more embedded processors (36), one or more embedded memory blocks (38), one or more embedded custom circuits (40), and a reconfigurable portion (42). An exemplary FPGA mentioned by Mukherjee is the Xilinx Virtex-Pro FPGA.

With regard to the language of claims 1, 2, 7, 16, 17 and 22, communications between Mukherjee's network nodes can be said to provide a "high bandwidth interconnection medium" forming a "reconfigurable communications infrastructure." Each of Mukherjee's network nodes, with its host machine (22) and associated one or more FPGA board blocks (24) provides an "ASIC device," however Mukherjee apparently does not specifically require that these network nodes perform a "packet router" function for the messages passed between nodes. Official Notice is taken that the usefulness of multiprocessor networks of the type wherein each network node acts as a "packet router" for inter-node messages was well known at the time the invention

was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement communication between Mukherjee's network nodes by means of a "packet router" function. Such an implementation would have been obvious because Mukherjee teaches that any type of inter-node interconnection arrangement can be used and because the usefulness of multiprocessor networks of the type wherein each network node acts as a "packet router" for inter-node messages was already well known.

Regarding claims 3, 8, 18, 23 and 34, Mukherjee suggests using the FPGA boards in various applications, such as remote drilling and space exploration vehicles (column 10, lines 26-39), presumably requiring a "signal processing" application for the FPGA boards.

Regarding claims 4, 5, 19, 20 and 31-33, Mukherjee suggests providing a fault tolerant multiprocessor architecture network and indicates that the disclosed software tool can be used to remove unneeded inter-node links, however Mukherjee does not specifically require that the network of nodes is a fully-connected network, *i.e.* that there is a direct duplex path between every pair of nodes. Official Notice is taken that the fault-tolerance advantage of multiprocessor networks wherein all network nodes are fully-connected was well-known at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement communication between Mukherjee's network nodes by means of a network that provides fully-connected nodes. Such an implementation would have been obvious because Mukherjee teaches that any type of inter-node interconnection arrangement

can be used and because the fault-tolerance advantage of multiprocessor networks wherein all network nodes are fully-connected was already well known.

Regarding claims 6 and 21, reconfigurable portions (42) of Mukherjee's FPGA boards provide "user-defined circuitry."

Regarding claims 9 and 24, FPGA boards of two different nodes can be considered "physically segregated."

Regarding claims 10, 27-29 and further regarding claims 31-33, using an "optical transmission medium" for the inter-node links is not specifically required by Mukherjee, although Mukherjee indicates that any type of interconnect medium can be considered. Official Notice is taken that the usefulness of an "optical transmission medium" for network links was well known at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement communication between Mukherjee's network nodes by means of an "optical transmission" network. Such an implementation would have been obvious because Mukherjee teaches that any type of inter-node interconnection arrangement can be used, and because the usefulness of an "optical transmission medium" for network links was already well known.

Regarding claim 11, using network links with a rate at least 1 Gbps is not specifically required by Mukherjee, although Mukherjee indicates that any type of interconnect medium can be considered. Official Notice is taken that the usefulness of a 1 Gbps or faster link for network communications was well known at the time the invention was made. It would have been obvious to a person having ordinary skill in the

art at the time the invention was made to implement communication between Mukherjee's network nodes by means of a 1 Gbps or faster link for network communications. Such an implementation would have been obvious because Mukherjee teaches that any type of inter-node interconnection arrangement can be used, and because the usefulness of a 1 Gbps or faster link for network communications was already well known.

Regarding claim 12, Mukherjee's software tool iteratively performs a process of scheduling, partitioning and mapping of "parallel tasks" to the FPGA boards (column 3, lines 43+).

Regarding claims 13-15, tasks can be mapped and re-mapped into one or more of the plural FPGA boards associated with one or more nodes of Mukherjee's network, and each of the one or more FPGA boards can be considered a "computing cluster" for the associated node, with each such "computing cluster" being capable of performing a separate "computing task" or sharing a task with one or more other computing clusters, however Mukherjee does not specifically describe the mapping and remapping of tasks to FPGA boards required by claims 13-15. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to apply Mukherjee's software tool to the configuring and reconfiguring of multiple tasks recited in claims 13-15. Such applications would have been obvious because according to Mukherjee tasks can be mapped and re-mapped into one or more of the plural FPGA boards associated with one or more nodes of Mukherjee's network.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen M. Baker whose telephone number is (571) 272-3814. The examiner can normally be reached on Monday-Friday (11:00 AM - 7:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Stephen M. Baker/
Primary Examiner
Art Unit 2112

smb

Notice of References Cited	Application/Control No. 11/600,934	Applicant(s)/Patent Under Reexamination YANCEY ET AL.	
	Examiner Stephen M. Baker	Art Unit 2112	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,802,290	09-1998	Casselman, Steven M.	709/201
*	B	US-5,931,959	08-1999	Kwiat, Kevin Anthony	714/48
*	C	US-6,339,819 B1	01-2002	Huppenthal et al.	712/16
*	D	US-6,614,267 B2	09-2003	Taguchi, Hideki	326/101
*	E	US-6,668,361 B2	12-2003	Bailis et al.	716/4
*	F	US-6,754,881 B2	06-2004	Kuhlmann et al.	716/16
*	G	US-7,389,487 B1	06-2008	Chan et al.	716/17
*	H	US-7,404,170 B2	07-2008	Schott et al.	716/16
*	I	US-7,415,331 B2	08-2008	Dapp et al.	701/25
*	J	US-7,439,763 B1	10-2008	Kavipurapu et al.	326/38
*	K	US-7,453,899 B1	11-2008	Vaida et al.	370/419
*	L	US-7,506,297 B2	03-2009	Mukherjee et al.	716/18
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11600934	YANCEY ET AL.
	Examiner	Art Unit
	Stephen M Baker	2112

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	06/18/2010								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								
	11	✓								
	12	✓								
	13	✓								
	14	✓								
	15	✓								
	16	✓								
	17	✓								
	18	✓								
	19	✓								
	20	✓								
	21	✓								
	22	✓								
	23	✓								
	24	✓								
	25	✓								
	26	✓								
	27	✓								
	28	✓								
	29	✓								
	30	✓								
	31	✓								
	32	✓								
	33	✓								
	34	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11600934	YANCEY ET AL.
	Examiner	**Art Unit**
	Stephen M Baker	2112

SEARCHED

Class	Subclass	Date	Examiner
714	4, 5	06/19/2010	SMB

SEARCH NOTES

Search Notes	Date	Examiner

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner

Form PTO-1449 (modified)

List of Patents and Publications for Applicant's

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty. Docket No.	Serial No.
LCOM:057	11/600,934
Applicant: JERRY YANCEY ET AL.	
Filing Date: 11/16/06	Group: 2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Page*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A57	7,224,184	5/29/07	Levi et al.			11/5/04

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation

Examiner:	/Stephen Baker/	Date Considered:	05/09/2010

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

Form PTO-1449 (modified)

List of Patents and Publications for Applicant's

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty. Docket No.	Serial No.
LCOM:057	11/600,934
Applicant: JERRY YANCEY ET AL.	
Filing Date: 11/16/06	Group: 2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Page*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A35	US2005/0169311A1	8/4/05	Millet et al.			1/29/04
	A36	7,137,048	11/14/06	Zerbe et al.			10/12/01
	A37	6,201,829	3/13/01	Schneider			4/3/98
	A38	6,385,236	5/7/02	Chen			10/5/98
	A39	5,953,372	9/14/99	Virzi			12/13/96
	A40	US2004/0158784A1	8/12/04	Abuhamdeh et al.			8/22/03
	A41	7,003,585	2/21/06	Phong et al.			9/5/01
	A42	6,020,755	2/1/00	Andrews et al.			9/26/97

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation

Examiner:	/Stephen Baker/	Date Considered:	05/09/2010

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

Form PTO-1449 (modified)

List of Patents and Publications for Applicant's

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty. Docket No.	Serial No.
LCOM:057	11/600,934
Applicant: JERRY YANCEY ET AL.	
Filing Date: 11/16/06	Group: 2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Page*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A55	7,260,650	8/21/07	Lueckenhoff			11/28/01

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation

Examiner:	/Stephen Baker/	Date Considered:	05/09/2010

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

Form PTO-1449 (modified)	Atty. Docket No. LCOM:057	Serial No. 11/600,934
List of Patents and Publications for Applicant's **INFORMATION DISCLOSURE STATEMENT** (Use several sheets if necessary)	Applicant JERRY YANCEY ET AL.	
	Filing Date: 11/16/06	Group: 2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Page 1*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A48	7,020,147	3/28/06	Amadon et al.			11/13/01
	A49	5,838,167	11/17/98	Erickson et al.			5/13/97
	A50	5,737,235	4/7/98	Kean et al.			9/6/95
	A51	US2005/0242 834A1	11/3/05	Vadi et al.			4/30/04

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C24	Search Report, PCT/US07/23700; April 18, 2008; 2 pgs.

Examiner:	/Stephen Baker/	**Date Considered:**	05/09/2010

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

IFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JERRY W. YANCEY ET AL.
Filed:	NOVEMBER 16, 2006
For:	RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS
Serial No.:	11/600,934
Group Art Unit:	2133
Examiner:	UNKNOWN
Atty Dkt:	LCOM:057

Pursuant to 37 C.F.R. 1.8, I certify that this correspondence is being deposited with the U.S. Postal Service in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313

8/1/07 — Date

Mary Gore — Name

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the document(s) listed on attached Form PTO-1449 be considered by the Examiner and made of record.

In accordance with 37 C.F.R §§ 1.97(g),(h), this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made, and is not to be construed to be an admission that (a) the information cited is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b); and/or (b) that the information cited is, or is considered to be prior art.

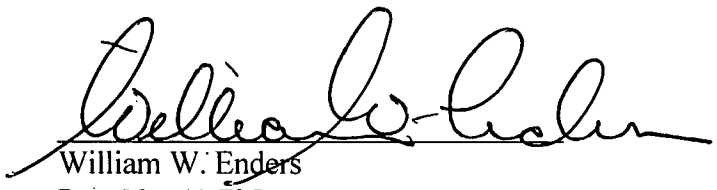
ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

The present Supplemental Information and Disclosure Statement is being filed prior to the receipt of a first Official Action reflecting an examination on the merits, and hence is believed to be timely filed in accordance with 37 C.F.R. § 1.97(b). No fees are believed to be due in connection with the filing of this Supplemental Information Disclosure Statement, however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to these materials, the Commissioner is hereby authorized to deduct said fees from Deposit Account No. 10-1205/LCOM:057.

A copy of the listed document(s) required by 37 C.F.R. § 1.98(a)(2) is enclosed for the convenience of the Examiner.

Applicant respectfully requests that the listed document(s) be made of record in the present case.

Respectfully submitted,



William W. Enders
Reg. No. 41,735
Attorney for Applicant

O'KEEFE, EGAN, PETERMAN & ENDERS, LLP
1101 Capital of Texas Highway South
Building C, Suite 200
Austin, Texas 78746
(512) 347-1611
FAX: (512) 347-1615

Enclosures

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

Form PTO-1449 (modified)

List of Patents and Publications for Applicant's

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty. Docket No.	Serial No.
LCOM:057	11/600,934
Applicant: JERRY YANCEY ET AL.	
Filing Date: 11/16/06	Group: 2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Page*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A30	6,381,238	4/30/02	Hluchyj			7/31/98
	A31	US2005/0248364A1	11/10/05	Vadi et al.			4/30/04
	A32	6,333,641	12/25/01	Wasson			5/5/00
	A33	US2005/0044439A1	2/24/05	Shatas et al.			9/10/04
	A34	6,888,376	5/3/05	Venkata et al.			9/24/03

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation

Examiner:	/Stephen Baker/	Date Considered:	05/09/2010

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JERRY W. YANCEY ET AL.
Filed:	NOVEMBER 16, 2006
For:	RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS
Serial No.:	11/600,934
Group Art Unit:	UNKNOWN
Examiner:	UNKNOWN
Atty Dkt:	LCOM:057

Pursuant to 37 C.F.R. 1.8, I certify that this correspondence is being deposited with the U.S. Postal Service in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313

Date 11/28/06 Name

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the document(s) listed on attached Form PTO-1449 be considered by the Examiner and made of record.

In accordance with 37 C.F.R §§ 1.97(g),(h), this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made, and is not to be construed to be an admission that (a) the information cited is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b); and/or (b) that the information cited is, or is considered to be prior art.

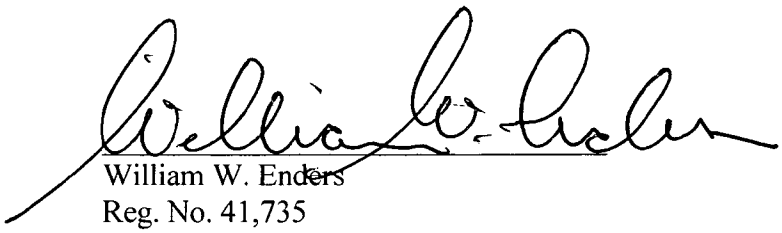
ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

The present Supplemental Information and Disclosure Statement is being filed prior to the receipt of a first Official Action reflecting an examination on the merits, and hence is believed to be timely filed in accordance with 37 C.F.R. § 1.97(b). No fees are believed to be due in connection with the filing of this Supplemental Information Disclosure Statement, however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to these materials, the Commissioner is hereby authorized to deduct said fees from Deposit Account No. 10-1205/LCOM:057.

A copy of the listed document(s) required by 37 C.F.R. § 1.98(a)(2) is enclosed for the convenience of the Examiner.

Applicant respectfully requests that the listed document(s) be made of record in the present case.

Respectfully submitted,



William W. Enders
Reg. No. 41,735
Attorney for Applicant

O'KEEFE, EGAN & PETERMAN, LLP
1101 Capital of Texas Highway South
Building C, Suite 200
Austin, Texas 78746
(512) 347-1611
FAX: (512) 347-1615

Enclosures

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

Form PTO-1449 (modified)

List of Patents and Publications for Applicant's

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty. Docket No. LCOM:057	Serial No. 11/600,934
Applicant JERRY YANCEY ET AL. .	
Filing Date: 11/16/06	Group: UNKNOWN

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page	*See Page*	*See Page 1*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A1						

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C23	Copending Patent Application Serial No. 11/600,935; LCOM:056, entitled "Methods And Systems For Relaying Data Packets", filed November 16, 2006; 101 pgs.

Examiner:	/Stephen Baker/	Date Considered:	05/09/2010

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

Form PTO-1449 (modified)

List of Patents and Publications for Applicant's

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty. Docket No.	Serial No.
LCOM:057	11/600,934
Applicant	
JERRY YANCEY ET AL.	
Filing Date:	**Group:**
11/16/06	2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Page*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A52	6,075,380	6/13/00	Lane			10/27/97
	A53	7,111,110	9/19/06	Pedersen			12/10/02
	A54	6,993,032	1/31/06	Dammann et al.			6/29/00

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation

Examiner:	/Stephen Baker/	Date Considered:	05/09/2010

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

Form PTO-1449 (modified)

List of Patents and Publications for Applicant's

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty. Docket No.	Serial No.
LCOM:057	11/600,934
Applicant: JERRY YANCEY ET AL.	
Filing Date: 11/16/06	Group: 2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Page*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A44	US2003/0026260A1	2/6/03	Ogasawara et al.			8/5/02
	A45	US2004/0240468A1	12/2/04	Chin et al.			5/30/03
	A46	US2003/0167340A1	9/4/03	Jonsson			5/17/01
	A47	US2004/0156368A1	8/12/04	Barri et al.			2/11/03

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation

Examiner:	/Stephen Baker/	Date Considered:	05/09/2010

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

Form PTO-1449 (modified)

List of Patents and Publications for Applicant's

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty. Docket No.	Serial No.
LCOM:057	11/600,934
Applicant: JERRY YANCEY ET AL.	
Filing Date: 11/16/06	Group: 2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Page*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A56	4,528,658	7/9/85	Israel			9/13/82

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation

Examiner:	/Stephen Baker/	Date Considered:	05/09/2010

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JERRY W. YANCEY ET AL.
Filed:	HEREWITH
For:	RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS
Serial No.:	UNKNOWN
Group Art Unit:	UNKNOWN
Examiner:	UNKNOWN
Atty Dkt:	LCOM:057

EXPRESS MAIL CERTIFICATION

NUMBER: EV978890499US

I hereby certify that this paper or fee is being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" service, postage prepaid, under 37 C.F.R. 1.10 on the date indicated below and is addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313.

Signature: Marty Jones — Date of Deposit: 11/16/06

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98, it is respectfully requested that this Information Disclosure Statement be entered and the document(s) listed on attached Form PTO-1449 be considered by the Examiner and made of record.

In accordance with 37 C.F.R §§ 1.97(g),(h), this Information Disclosure Statement is not to be construed as a representation that a search has been made, and is not to be construed to be an admission that (a) the information cited is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b); and/or (b) that the information cited is, or is considered to be prior art.

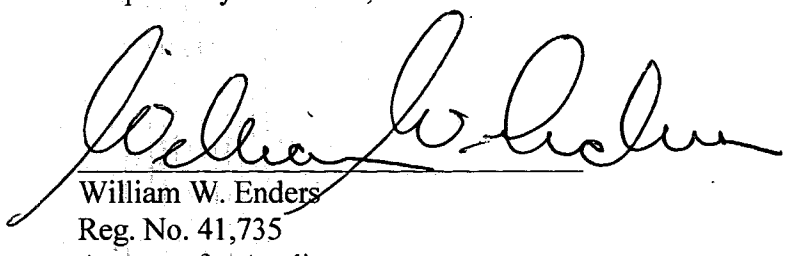
ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

The present Information and Disclosure Statement is being filed prior to the receipt of a first Official Action reflecting an examination on the merits, and hence is believed to be timely filed in accordance with 37 C.F.R. § 1.97(b). No fees are believed to be due in connection with the filing of this Information Disclosure Statement, however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to these materials, the Commissioner is hereby authorized to deduct said fees from Deposit Account No. 10-1205/LCOM:057.

A copy of the listed document(s) required by 37 C.F.R. § 1.98(a)(2) is enclosed for the convenience of the Examiner.

Applicant respectfully requests that the listed document(s) be made of record in the present case.

Respectfully submitted,



William W. Enders
Reg. No. 41,735
Attorney for Applicant

O'KEEFE, EGAN & PETERMAN, LLP
1101 Capital of Texas Highway South
Building C, Suite 200
Austin, Texas 78746
(512) 347-1611
FAX: (512) 347-1615

Enclosures

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

Form PTO-1449 (modified)	Atty. Docket No. LCOM:057	Serial No. UNKNOWN
List of Patents and Publications for Applicant's	Applicant JERRY YANCEY ET AL. .	
INFORMATION DISCLOSURE STATEMENT	Filing Date: HEREWITH	Group: UNKNOWN
(Use several sheets if necessary)		

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Pages 1-3*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A1	6,617,877	9/9/03	Cory et al.			3/1/02
	A2	6,651,225	11/18/03	Lin et al.			4/10/00
	A3	6,421,251	7/16/02	Lin			2/5/98
	A4	6,389,379	5/14/02	Lin et al.			6/12/98
	A5	US2005/0256 969A1	11/17/05	Yancey et al.			5/11/04
	A6	6,496,291	12/17/02	Raj et al.			10/17/00
	A7	US2002/0095 400A1	7/18/02	Johnson et al.			6/12/01
	A8	US2002/0059 274A1	5/16/02	Hartsell et al.			6/12/01
	A9	6,901,072	5/31/05	Wong			5/15/03

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C1	Laxdal, "ELEC 563 Project Reconfigurable Computers", http://www.ece.uvic.ca/~elaxdal/Elec563/reconfigurable_computers.html; printed from the Internet December 19, 2003, December 2, 1999, 10 pgs.
	C2	"PCI/DSP-4 Four Complete Channels Of Digital Acoustic Emission Data Acquisition On A Single Board", http://www.pacndt.com/products/Multichannel/pcidsp.html, printed from the Internet December 19, 2003, 3 pgs.

Examiner: /Stephen Baker/	**Date Considered:** 05/09/2010

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

Form PTO-1449 (modified)	Atty. Docket No. LCOM:057	Serial No. UNKNOWN
List of Patents and Publications for Applicant's **INFORMATION DISCLOSURE STATEMENT** (Use several sheets if necessary)	Applicant JERRY YANCEY ET AL. .	
	Filing Date: HEREWITH	Group: UNKNOWN

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Pages 1-3*

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C3	Zaiq Technologies, "Innovation: Methodology Briefs", http://www.zaiqtech.com/innovation/m_fpga.html, printed from the Internet January 15, 2004, 12 pgs.
	C4	Hardt et al, "Flysig: Dataflow Oriented Delay-Insensitive Processor For Rapid Prototyping Of Signal Processing", (obtained from Internet December, 2003), 6 pgs.
	C5	Chang et al., "Evaluation Of Large Matrix Operations On A Reconfigurable Computing Platform For High Performance Scientific Computations," (obtained from Internet December, 2003), 10 pgs.
	C6	Alfke, "FPGA Configuration Guidelines," XAPP, 090 November 24, 1997, Version 1.1, pps. 31-38.
	C7	"XC18V00 Series Of In-System Programmable Configuration PROMs", Xilinx Product Specification, DS026 (v.3.0), November 12, 2001, 19 pgs.
	C8	Thacker, "System ACE Technology: Configuration Manager Breakthrough", New Technology, FPGA Configuration, Xcell Journal, Summer 2001, pps. 52-55.
	C9	"System ACE MPM Solution", Xilinx Product Specification, DS087 (v1.0) September 25, 2001, 29 pgs.
	C10	"RapidIO™: An Embedded System Component Network Architecture", Architecture And Systems Platforms, February 22, 2000, 25 pgs.
	C11	"Raceway Internlink Functional Specification", Mercury Computer Systems, Inc., November 8, 2000, 118 pgs.
	C12	"[XMC-3310] High Speed Transceiver ePMC Module", Spectrum Signal Processing, http://www.spectrumsignal.com/Products/_Datasheets/XMC-3310_datasheet.asp, (©2002-2004), 5 pgs. (this reference describes a product available prior to the May 11, 2004 filing date of the present application)
	C13	"XMC-3310 High Speed Transceiver ePMC Module", Spectrum Signal Processing, Rev. May, 2004, 4 pgs. (this reference describes a product available prior to the May 11, 2004 filing date of the present application)
	C14	RocketIO™ Transceiver User Guide, Xilinx, UG024 (v2.3) February 24, 2004, 152 pgs.
	C15	"The FPGA Systems Connectivity Tool", Product Brief, Nallatech, DIMEtalk 2.1, February 2004, pps 1-8.

Examiner: /Stephen Baker/	**Date Considered:** 05/09/2010

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

Form PTO-1449 (modified)	Atty. Docket No. LCOM:057	Serial No. UNKNOWN
List of Patents and Publications for Applicant's **INFORMATION DISCLOSURE STATEMENT** (Use several sheets if necessary)	Applicant JERRY YANCEY ET AL. .	
	Filing Date: HEREWITH	Group: UNKNOWN

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Pages 1-3*

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C16	B. Hall, "BTeV Front End Readout & Links", BTEV Co., August 17, 2000, 11 pgs.
	C17	Irwin, "Usage Models For Multi-Gigabit Serial Transceivers", Xilinx, xilinix.com, White Paper, WP157 (v1.0), March 15, 2002, 10 pgs.
	C18	Campenhout, "Computing Structures And Optical Interconnect: Friends Or Foes?", Department of Electronics And Information Systems, Ghent University, Obtained from Internet October 8, 2006, 11 pgs.
	C19	E. Hazen, "HCAL HO Trigger Link", Optical SLB-HTR Interface Specification, May 24, 2006, 4 pgs.
	C20	G. Russell, "Analysis And Modelling Of Optically Interconnected Computing Systems", School of Engineering And Physical Sciences, Heriot-Watt University, May 2004, 170 pgs.
	C21	Copending Patent Application Serial No. 11/529,712; LCOM:011C1, entitled "Systems And Methods For Interconnection Of Multiple FPGA Devices", filed September 28, 2006; 42 pgs.
	C22	Copending Patent Application Serial No. 11/529,713; LCOM:011C2, entitled "Systems And Methods For Interconnection Of Multiple FPGA Devices", filed September 28, 2006; 42 pgs.

Examiner: /Stephen Baker/	**Date Considered:** 05/09/2010

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 4821

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
11/600,934	11/16/2006	714	2112	LCOM:057

APPLICANTS

Jerry W. Yancey, Rockwall, TX;
Yea Zong Kuo, Rockwall, TX;

**** CONTINUING DATA ***************************

This application is a CIP of 10/843,226 05/11/2004 PAT 7,444,454

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

12/07/2006

Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged	Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ Yes ☑ No	☐ Yes ☑ No	/STEPHEN M BAKER/ Examiner's Signature	☐ Initials	TX	18	34	4

ADDRESS

O'KEEFE, EGAN, PETERMAN & ENDERS LLP
1101 CAPITAL OF TEXAS HIGHWAY SOUTH
#C200
AUSTIN, TX 78746
UNITED STATES

TITLE

Reconfigurable communications infrastructure for ASIC networks

FILING FEE RECEIVED		
2030	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Form PTO-1449 (modified)

List of Patents and Publications for Applicant's

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty. Docket No.	Serial No.
LCOM:057	11/600,934
Applicant: JERRY YANCEY ET AL.	
Filing Date: 11/16/06	Group: 2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page 1*	*See Page*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A43	6,233,704	5/15/01	Scott et al.			3/13/96

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1	GB2377138A	12/31/02	United Kingdom			Yes

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation

Examiner:	/Stephen Baker/	Date Considered:	05/09/2010

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JERRY W. YANCEY ET AL.
Filed:	NOVEMBER 16, 2006
For:	RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS
Serial No.:	11/600,934
Group Art Unit:	2133
Examiner:	UNKNOWN
Atty Dkt:	LCOM:057

Pursuant to 37 C.F.R. 1.8, I certify that this correspondence is being deposited with the U.S. Postal Service in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313

6/5/07 — Date

Name

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the document(s) listed on attached Form PTO-1449 be considered by the Examiner and made of record.

In accordance with 37 C.F.R §§ 1.97(g),(h), this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made, and is not to be construed to be an admission that (a) the information cited is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b); and/or (b) that the information cited is, or is considered to be prior art.

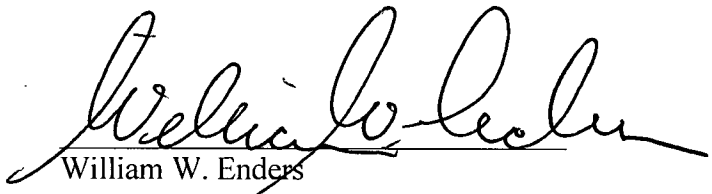
ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

The present Supplemental Information and Disclosure Statement is being filed prior to the receipt of a first Official Action reflecting an examination on the merits, and hence is believed to be timely filed in accordance with 37 C.F.R. § 1.97(b). No fees are believed to be due in connection with the filing of this Supplemental Information Disclosure Statement, however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to these materials, the Commissioner is hereby authorized to deduct said fees from Deposit Account No. 10-1205/LCOM:057.

A copy of the listed document(s) required by 37 C.F.R. § 1.98(a)(2) is enclosed for the convenience of the Examiner.

Applicant respectfully requests that the listed document(s) be made of record in the present case.

Respectfully submitted,



William W. Enders
Reg. No. 41,735
Attorney for Applicant

O'KEEFE, EGAN, PETERMAN & ENDERS, LLP
1101 Capital of Texas Highway South
Building C, Suite 200
Austin, Texas 78746
(512) 347-1611
FAX: (512) 347-1615

Enclosures

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

Form PTO-1449 (modified)

List of Patents and Publications for Applicant's

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Atty. Docket No.	Serial No.
LCOM:057	11/600,934
Applicant	
JERRY YANCEY ET AL. .	
Filing Date:	**Group:**
11/16/06	2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Pages 1-2	*See Page*	*See Page*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A10	7,035,228	4/25/06	Baumer			10/29/03
	A11	US2005/0183 042A1	8/18/05	Vogel et al.			12/2/03
	A12	6,721,313	4/13/04	Van Duyne			8/1/00
	A13	6,259,693	7/10/01	Ganmukhi et al.			8/28/97
	A14	US2004/0249 964A1	12/9/04	Mougel			3/6/03
	A15	US2004/0085 902A1	5/6/04	Miller et al.			3/5/03
	A16	6,172,927	1/9/01	Taylor			3/24/00
	A17	6,965,571	11/15/05	Webber			8/27/01
	A18	7,188,283	3/6/07	Shafer et al.			9/11/03
	A19	6,292,923	9/18/01	Genrich et al.			3/24/00
	A20	US2004/0131 072A1	7/8/04	Khan et al.			8/12/03
	A21	6,873,180	3/29/05	Bentz			3/24/03
	A22	5,941,988	8/24/99	Bhagwat et al.			1/27/97
	A23	6,496,505	12/17/02	La Porta et al.			12/11/98
	A24	6,934,763	8/23/05	Kubota et al.			3/21/01
	A25	US2002/0021 680A1	2/21/02	Chen			7/30/01
	A26	US2002/0057 657A1	5/16/02	La Porta et al.			12/11/98
	A27	US2003/0009 585A1	1/9/03	Antoine et al.			12/17/01
	A28	US2005/0175 018A1	8/11/05	Wong			11/29/04

Examiner: /Stephen Baker/ **Date Considered:** 05/09/2010

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

Form PTO-1449 (modified)	Atty. Docket No. LCOM:057	Serial No. 11/600,934
List of Patents and Publications for Applicant's **INFORMATION DISCLOSURE STATEMENT** (Use several sheets if necessary)	Applicant JERRY YANCEY ET AL. .	
	Filing Date: 11/16/06	Group: 2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Pages 1-2	*See Page*	*See Page*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A29	US2006/0002386A1	1/5/06	Yik et al.			6/30/04

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation

Examiner: /Stephen Baker/	**Date Considered:** 05/09/2010

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JERRY W. YANCEY ET AL.
Filed:	NOVEMBER 16, 2006
For:	RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS
Serial No.:	11/600,934
Group Art Unit:	2112
Examiner:	BAKER, STEPHEN M.
Atty Dkt:	LCOM:057

Pursuant to 37 C.F.R. 1.8, I certify that this correspondence is being deposited with the U.S. Postal Service in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313 on the date below:

10/25/10 [signature]
Date Name

Commissioner For Patents
P. O. Box 1450
Alexandria, VA 22313

I. AMENDMENT; and

II. RESPONSE TO OFFICE ACTION DATED JUNE 23, 2010

Sir:

This paper is submitted in response to the Office Action dated June 23, 2010.

A Request For Extension Of Time To Respond To Office Action Dated June 23, 2010 is being filed concurrently herewith.

Reconsideration of the application is respectfully requested.

I. AMENDMENT

In the Specification:

Please amend paragraph 0099 as follows:

[0099] Reconfigurable communications infrastructure 1300 of Figures 13-15 may be configured in one exemplary embodiment with a PRISM routing scheme that provides a duplex data communication link between each FPGA of a given signal processing circuit (*e.g.*, circuit card) and high bandwidth interface 1510 (*e.g.*, PMC interface site 124 of Figure 1) with high bandwidth interconnection medium 1350. In such a configuration, a data packet may be routed from a given source of a source computing device (*e.g.*, FPGA 1320) of a first reconfigurable signal processing circuit to a given destination of a destination computing device (*e.g.*, a different FPGA 1320) of a second reconfigurable signal processing circuit using, for example, PRISM router and data packet configurations illustrated and described herein in relation to Figures 5, 6 and 7. However, it will be understood that any other data packet configuration and routing scheme suitable for allowing a sender or source to determine the packet's destination within a reconfigurable communications infrastructure 1300 may be employed (*e.g.*, TCP/IP, Fibrechannel, XAUI, Ethernet, Infiniband, Rapid I/O, *etc.*). Further information on exemplary methodology and systems that may be employed for relaying data packets in the disclosed systems and methods may be found in United States Patent Application Serial No. [[_____]] 11/600,935, entitled "METHODS AND SYSTEMS FOR RELAYING DATA PACKETS" by Yancey, et al. (Atty. Docket LCOM-056) filed on the same date as the present application and which is incorporated herein by reference.

In the Claims:

Please amend claims 1-24, 27, 29-31 and 33-34 as follows. This listing of claims will replace all prior versions, and listings, of claims for the present application:

1. (Currently Amended) A method, comprising:

providing two or more separate signal processing circuits, each one of said two or more signal processing circuits including multiple ASIC devices that each includes ~~ASIC devices, each one of said two or more ASIC devices comprising~~ a respective packet router;

providing a high bandwidth interconnection medium coupled between said signal processing circuits ~~packet routers of each of said two or more ASIC devices~~ to form a reconfigurable communications infrastructure of said two or more signal processing circuits, the two or more signal processing circuits being selectively segregatable from each other, and the respective ASIC devices of each one of said two or more signal processing circuits being directly coupled to said high bandwidth interconnection medium by a respective common interface provided for the ASIC devices of each of said two or more signal processing circuits with no other processing device intervening between the high bandwidth interconnection medium and said respective ASIC devices; and

selectively communicating data between said two or more signal processing circuits by selectively routing data through the packet router ~~routers~~ of each of the respective ASIC devices of each one of said signal processing circuits ~~two or more ASIC devices~~ across ~~said~~ a first common interface to the high bandwidth interconnection medium and to an other one of said signal processing circuits through a second common interface to the packet router of each of the respective

ASIC devices of said other one of said signal processing circuits without routing said data through any other intervening processing device between each respective ASIC device and the high bandwidth interconnection medium.

2. (Currently Amended) The method of claim 1, wherein each of said ~~two or more~~ ASIC devices of said two or more signal processing circuits is an FPGA device ~~comprises FPGA devices~~.

3. (Currently Amended) The method of claim 9 [[2]], wherein said two or more signal processing circuits are physically segregated from each other by at least one of being positioned in different rooms of a given building or facility from each other, or being positioned in different compartments of a given mobile vehicle from each other ~~further comprising:~~

~~providing said two or more FPGA devices by providing two or more signal processing circuits, each one of said two or more signal processing circuits comprising at least one FPGA device that comprises a packet router;~~

~~providing said high bandwidth interconnection medium coupled between said two or more signal processing circuits to provide data communication between said packet routers of said FPGA devices of each of said two or more signal processing circuits; and~~

~~communicating data across said high bandwidth interconnection medium between said packet routers of said FPGA devices of each of said two or more signal processing circuits~~.

4. (Currently Amended) The method of claim 2 [[3]], wherein ~~at least one of~~ each of said signal processing circuits is a reconfigurable signal processing circuit that ~~further~~ comprises two or

more FPGA devices that each ~~comprise~~ includes a packet router, said packet router of each one of said two or more FPGA devices of each given one of said ~~at least one~~ signal processing circuits ~~circuit~~ being coupled to each respective packet router of each of the other of said two or more FPGA devices of said ~~at least one~~ same given one of said signal processing circuits ~~circuit~~; and wherein said method further comprises using said packet router of each given one of said two or more FPGA devices of each given one of said ~~at least one~~ signal processing circuits ~~circuit~~ to communicate data packets within said given signal processing circuit by routing data packets to and from ~~with~~ each other of said two or more FPGA devices of the same given one of said ~~at least one~~ signal processing circuits ~~circuit~~ without routing said data packets outside said given signal processing circuit across said first or second common interfaces to said high bandwidth interconnection medium.

5. (Currently Amended) The method of claim 4, wherein said packet router of each one of said two or more FPGA devices of each given one of said ~~at least one~~ signal processing circuits ~~circuit~~ is coupled to each respective packet router of each of the other of said two or more FPGA devices of same said ~~at least one~~ same given one of said signal processing circuits ~~circuit~~ by a separate respective duplex data communication link so as to form a direct serial interconnection between each two of said two or more FPGA devices of said same given one of said signal processing circuits ~~circuit~~; and wherein said method further comprises using said packet router of each given one of said two or more FPGA devices of said each given one of said ~~at least one~~ signal processing circuits ~~circuit~~ to transmit and receive data packets across each of said separate respective duplex data communication links existing between said given one of said two or more FPGA devices and each other of said two or more FPGA devices of the same given one of said ~~at least one~~ signal processing circuits ~~circuit~~ without routing said data packets outside said given signal processing circuit across said first or second common interfaces to said high bandwidth interconnection medium.

6. (Currently Amended) The method of claim 2, wherein each given one of said ~~two or more~~ FPGA devices of one of said signal processing circuits comprises user-defined circuitry coupled

to said respective packet router of said given one of said ~~two or more~~ FPGA devices; and wherein said method further comprises transmitting and receiving data packets between said user-defined circuitry of said given one of said ~~two or more~~ FPGA devices of one of said signal processing circuits and an other one of said FPGA devices of an other different one of said signal processing circuits across said first and second common interfaces and through said high bandwidth interconnection medium.

7. (Currently Amended) The method of claim 2, wherein each given one of said ~~two or more~~ FPGA devices of one of said signal processing circuits comprises at least one embedded processor coupled to said respective packet router of said given one of said ~~two or more~~ FPGA devices; and wherein said method further comprises transmitting and receiving data packets between said at least one embedded processor of said given one of said ~~two or more~~ FPGA devices of one of said signal processing circuits and an other one of said FPGA devices of an other different one of said signal processing circuits across said first and second common interfaces and through said high bandwidth interconnection medium.

8. (Currently Amended) The method of claim 2, further comprising providing a vehicle-based reconfigurable communications infrastructure comprising a vehicle with each of said two or more ~~FPGA devices~~ signal processing circuits and said high bandwidth interconnection medium being positioned on or within said vehicle; and communicating data between said two or more signal processing circuits through said packet routers of each of said ~~two or more~~ FPGA devices of said two or more signal processing circuits across said first and second common interfaces and through said high bandwidth interconnection medium on or within said vehicle.

9. (Currently Amended) The method of claim 2, further comprising providing said two or more signal processing circuits ~~FPGA devices~~ in positions physically segregated from each other; and communicating data between said packet router ~~routers~~ of a respective one said FPGA devices of each of said two or more physically-segregated signal processing circuits ~~FPGA devices~~ across

said first and second common interfaces and through said high bandwidth interconnection medium to the packet router of a respective FPGA device of an other one of said signal processing circuits without routing said data through any other intervening processing device between each respective FPGA device and the high bandwidth interconnection medium.

10. (Currently Amended) The method of claim 2, wherein said high bandwidth interconnection medium comprises an optical transmission medium; and wherein said method further comprises selectively communicating data between said two or more signal processing circuits by selectively routing data through the packet router ~~routers~~ of a respective FPGA device of each one of said two or more signal processing circuits ~~FPGA devices~~ across said first and second common interfaces and through said optical transmission medium to a respective FPGA device of an other different one of said signal processing circuits without routing said data through any other intervening processing device between each respective FPGA device and the high bandwidth interconnection medium.

11. (Currently Amended) The method of claim 2, further comprising selectively communicating data between said two or more signal processing circuits by selectively routing data through the packet router ~~routers~~ of a respective FPGA device of each one of said two or more signal processing circuits ~~FPGA devices~~ at a data transmission rate of greater than or equal to about 1 Gbps to a respective FPGA device of an other different one of said signal processing circuits without routing said data through any other intervening processing device between each respective FPGA device and the high bandwidth interconnection medium.

12. (Currently Amended) The method of claim 2, further comprising configuring each of said at least two separate signal processing circuits ~~FPGA devices~~ to perform different computing tasks in parallel.

13. (Currently Amended) The method of claim 2, further comprising:

providing said two or more separate signal processing circuits ~~FPGA devices~~ as a first signal processing circuit ~~first~~ and a second signal processing circuit ~~FPGA devices~~;

configuring said first and second signal processing circuits ~~FPGA devices~~ to perform a first computing task together as a first computing cluster;

providing at least two additional separate signal processing circuits ~~FPGA devices~~ as a third signal processing circuit including multiple FPGA devices and a fourth signal processing circuit including multiple FPGA devices, the first, second, third and fourth signal processing circuits being selectively segregatable from each other and each one of said respective FPGA devices of said third and fourth signal processing circuits ~~FPGA devices comprising a packet router~~ being directly coupled to said high bandwidth interconnection medium by a respective common interface provided for the FPGA devices of each of said third and fourth signal processing circuits with no other processing device intervening between the high bandwidth interconnection medium and the FPGA devices of said respective third and fourth signal processing circuits;

dynamically configuring said third and fourth separate signal processing circuits ~~FPGA devices~~ in real time to perform a second computing task together as a second computing cluster, said second computing task being different than said first computing task; and

simultaneously performing said first computing task with said first computing cluster and said second computing task with said second computing cluster.

14. (Currently Amended) The method of claim 13, further comprising:

dynamically reconfiguring said first and third separate signal processing circuits ~~FPGA devices~~ in real time to perform a third computing task together as a third computing cluster;

dynamically configuring said second and fourth separate signal processing circuits ~~FPGA devices~~ in real time to perform a fourth computing task together as a fourth computing cluster, said fourth computing task being different than said third computing task; and

simultaneously performing said third computing task with said third computing cluster and said fourth computing task with said fourth computing cluster.

15. (Currently Amended) The method of claim 13, further comprising:

dynamically reconfiguring said first, second, third and fourth separate signal processing circuits ~~FPGA devices~~ in real time to perform a third computing task together as a third computing cluster; and

performing said third computing task with said third computing cluster.

16. (Currently Amended) A reconfigurable communications infrastructure, comprising:

two or more separate signal processing circuits, each one of said two or more signal processing circuits including at multiple ASIC devices that each includes ~~ASIC devices, each one of said two or more ASIC devices comprising~~ a respective packet router; and

a high bandwidth interconnection medium coupled between said signal processing circuits ~~packet routers of each of said two or more ASIC devices~~ to form said reconfigurable communications infrastructure of said two or more signal processing circuits, the two or more signal processing circuits being selectively segregatable from each other, and the respective ASIC devices of each one of said two or more signal processing circuits being directly coupled to said high bandwidth interconnection medium by a common interface provided for the ASIC devices of each of said two or more signal processing circuits with no other processing device intervening between the high bandwidth interconnection medium and said respective ASIC devices; and

wherein the reconfigurable communications infrastructure is configured to selectively communicate data between said two or more signal processing circuits by selectively routing data through the packet router of each of the respective ASIC devices of each one of said signal processing circuits across a first common interface said high bandwidth interconnection medium to an other one of said signal processing circuits through a second common interface to the packet router of each of the respective ASIC devices of said other one of said signal processing circuits without routing said data through any other intervening processing device between each respective ASIC device and the high bandwidth interconnection medium ~~provide data communication between said packet routers of each of said two or more ASIC devices~~.

17. (Currently Amended) The reconfigurable communications infrastructure of claim 16, wherein each of said ~~two or more~~ ASIC devices of said two or more signal processing circuits is an FPGA device ~~comprises FPGA devices~~.

18. (Currently Amended) The reconfigurable communications infrastructure of claim 24 ~~17~~, wherein said two or more signal processing circuits are physically segregated from each other by

at least one of being positioned in different rooms of a given building or facility from each other, or being positioned in different compartments of a given mobile vehicle from each other ~~further comprising:~~

~~two or more signal processing circuits, each one of said two or more signal processing circuits comprising at least one FPGA device that comprises a packet router; and~~

~~wherein said high bandwidth interconnection medium is coupled between said two or more signal processing circuits to provide data communication between said packet routers of said FPGA devices of each of said two or more signal processing circuits~~.

19. (Currently Amended) The reconfigurable communications infrastructure of claim 17 ~~18~~, wherein ~~at least one~~ each of said signal processing circuits is a reconfigurable signal processing circuit that ~~further~~ comprises two or more FPGA devices that each ~~comprise~~ includes a packet router, said packet router of each one of said two or more FPGA devices of each given on of said ~~at least one~~ signal processing ~~circuit~~ circuits being coupled to each respective packet router of each of the other of said two or more FPGA devices of said same given one of said ~~at least one~~ signal processing circuits ~~circuit~~; and wherein said packet router of each given one of said two or more FPGA devices of said signal processing circuits is configured to communicate data packets within said given signal processing circuit by routing data packets to and from each other of said two or more FPGA devices of the same given one of said signal processing circuits without routing said data packets outside said given signal processing circuit across said first or second common interfaces to said high bandwidth interconnection medium.

20. (Currently Amended) The reconfigurable communications infrastructure of claim 19, wherein said packet router of each one of said two or more FPGA devices of each given one of said ~~at least one~~ signal processing circuits ~~circuit~~ is coupled to each respective packet router of each of the other of said two or more FPGA devices of same said ~~at least one~~ same given one of

said signal processing ~~circuit~~ circuits by a separate respective duplex data communication link so as to form a direct serial interconnection between each two of said two or more FPGA devices of said same given one of said signal processing circuits ~~circuit~~; and wherein said packet router of each given one of said two or more FPGA devices of each given one of said signal processing circuits is configured to communicate data packets within said given signal processing circuit by routing data packets to and from each other of said two or more FPGA devices of the same given one of said signal processing circuits without routing said data packets outside said given signal processing circuit across said first or second common interfaces to said high bandwidth interconnection medium.

21. (Currently Amended) The reconfigurable communications infrastructure of claim 17, wherein each given one of said ~~two or more~~ FPGA devices of one of said signal processing circuits comprises user-defined circuitry coupled to said respective packet router of said given one of said ~~two or more~~ FPGA devices; and wherein said respective packet router of each given one of said ~~two or more~~ FPGA devices of one of said signal processing circuits is configured to transmit and receive data packets between said user-defined circuitry of said given one of said ~~two or more~~ FPGA devices of one of said signal processing circuits and an other one of said FPGA devices of an other different one of said signal processing circuits across said first and second common interfaces and through said high bandwidth interconnection medium.

22. (Currently Amended) The reconfigurable communications infrastructure of claim 17, wherein each given one of said ~~two or more~~ FPGA devices of one of said signal processing circuits comprises at least one embedded processor coupled to said respective packet router of said given one of said ~~two or more~~ FPGA devices; and wherein said respective packet router of each given one of said ~~two or more~~ FPGA devices of one of said signal processing circuits is configured to transmit and receive data packets between said at least one embedded processor of said given one of said ~~two or more~~ FPGA devices of one of said signal processing circuits and an other one of said FPGA devices of an other different one of said signal processing circuits across

said first and second common interfaces and through said high bandwidth interconnection medium.

23. (Currently Amended) The reconfigurable communications infrastructure of claim 17, wherein said reconfigurable communications infrastructure is a vehicle-based reconfigurable communications infrastructure comprising a vehicle; and wherein each of said two or more ~~FPGA devices~~ signal processing circuits, first and second common interfaces, and said high bandwidth interconnection medium is positioned on or within said vehicle.

24. (Currently Amended) The reconfigurable communications infrastructure of claim 17, wherein said two or more ~~FPGA devices~~ signal processing circuits are physically segregated from each other.

25. (Original) The reconfigurable communications infrastructure of claim 17, wherein said high bandwidth interconnection medium comprises an optical transmission medium.

26. (Original) The reconfigurable communications infrastructure of claim 17, wherein said high bandwidth interconnection medium comprises an interconnection medium having a data transmission capability of greater than or equal to about 1 Gbps.

27. (Currently Amended) A communications infrastructure, comprising two or more ~~ASIC devices~~ separate signal processing circuits, each one of said two or more ~~ASIC devices~~ signal processing circuits including multiple ASIC devices that each itself includes ~~comprising~~ a packet router, said packet router of each one of said ~~two or more~~ ASIC devices of each given one of said respective two or more signal processing circuits being coupled through respective first and second common interfaces and an intervening high speed serial optical link to a ~~each~~ respective

packet router of each of the ASIC devices of each other of said two or more ~~ASIC devices~~ signal processing circuits ~~by an interconnection comprising a high speed serial optical link~~ with no other processing device intervening between the high speed optical link and said ASIC devices of each of said two or more signal processing circuits.

28. (Original) The communications infrastructure of claim 27, wherein said interconnection further comprises a high bandwidth interconnection medium.

29. (Currently Amended) The communications infrastructure of claim 28, wherein each of said ~~two or more~~ the ASIC devices of said two or more signal processing circuits is an FPGA device ~~comprises FPGA devices~~.

30. (Currently Amended) The communications infrastructure of claim 27 ~~29~~, wherein said two or more signal processing circuits are physically segregated from each other by at least one of being positioned in different rooms of a given building or facility from each other, or being positioned in different compartments of a given mobile vehicle from each other ~~further comprising:~~

~~two or more signal processing circuits, each one of said two or more signal processing circuits comprising at least one FPGA device that comprises a packet router; and~~

~~wherein said interconnection is coupled between said two or more signal processing circuits to provide data communication between said packet routers of said FPGA devices of each of said two or more signal processing circuits~~.

31. (Currently Amended) A method, comprising:

providing two or more ~~ASIC devices~~ separate signal processing circuits, each one of said two or more ~~ASIC devices~~ signal processing circuits including multiple ASIC devices that each itself includes ~~comprising~~ a packet router, said packet router of each one of said ASIC devices of each given one of said respective two or more signal processing circuits being coupled through respective first and second common interfaces and an intervening high speed serial optical link to a respective packet router of each of the other ASIC devices of each other of said two or more signal processing circuits ~~coupled together~~ ~~by an interconnection comprising a high speed serial optical link~~ with no other processing device intervening between the high speed serial optical link and said ASIC devices of each of said two or more signal processing circuits, and

selectively transferring at least one data packet from each said packet router of each one of said ASIC devices of each given one of said respective two or more signal processing circuits ~~ASIC devices~~ to each respective packet router of said at ASIC devices of each of the other of said two or more signal processing circuits ~~ASIC devices~~ through said first and second common interfaces and said intervening ~~by said~~ high speed serial optical link without routing said data through any other intervening processing device between each respective ASIC device and the high speed serial optical link.

32. (Original) The method of claim 31, wherein said interconnection further comprises a high bandwidth interconnection medium.

33. (Currently Amended) The method of claim 32, wherein each of said ~~two or more~~ ASIC devices of said two or more signal processing circuits is an FPGA device ~~comprises FPGA devices~~.

34. (Currently Amended) The method of claim 31 ~~33~~, ~~further comprising:~~ wherein said two or more signal processing circuits are physically segregated from each other by at least one of being positioned in different rooms of a given building or facility from each other, or being positioned in different compartments of a given mobile vehicle from each other

~~providing said two or more FPGA devices by providing two or more signal processing circuits, each one of said two or more signal processing circuits comprising at least one FPGA device that comprises a packet router;~~

~~providing said interconnection coupled between said two or more signal processing circuits to provide data communication between said packet routers of said FPGA devices of each of said two or more signal processing circuits; and~~

~~communicating data across said interconnection between said packet routers of said FPGA devices of each of said two or more signal processing circuits~~.

II. RESPONSE TO OFFICE ACTION

Claims 1-24, 27, 29-31 and 33-34 have been amended to even more particularly point out and claim the subject matter of the claims. Claims 1-34 are pending.

A. The Objections to the Specification

Paragraph 0099 has been amended to address the objection regarding copending application data.

Contrary to the assertion in the Office Action, the terms "ASIC" and "FPGA" are used in an appropriate manner in the Specification, for example, in paragraph 0010 of the Specification which states that "[e]xamples of ASIC devices that may be interconnected using the disclosed systems and methods include, but are not limited to, Field Programmable Gate Arrays ("FPGAs") or other field programmable devices ("FPDs") or programmable logic devices ("PLDs")."

As evidence that FPGAs, FPDs and PLDs are each types of ASIC devices, Applicants submit herewith the attached definition of the term "ASIC" as Exhibit A. As clearly shown on page 2 of Exhibit A, the term "ASIC" embraces field programmable devices such as FPGAs. Each of the paragraphs of the Specification identified on page 2 of the Office Action uses these terms in a manner consistent with this definition. Thus, the usage of these terms in the Specification is entirely proper, and the objection to the Specification should be withdrawn.

Favorable reconsideration is requested.

B. The 35 USC Section 112 Rejections

Contrary to the rejections of the claims made on pages 2-3 of the Office Action, the usage of "ASIC devices" in these claims is clear (*see* Exhibit A and the discussion above regarding the objections to the Specification). Moreover, Applicants note that "it is a fundamental principal

that Applicants may be their own lexicographers, and that they "can define in the claims what they regard as their invention essentially in whatever terms they choose" and "a claim may not be rejected solely because of the type of language used to define the subject matter for which patent protection is sought" (*see* MPEP 2173.01). However, in the present case, the language of Applicants' claims is already consistent with the definition of the term "ASIC", and is thus completely acceptable for this reason alone.

Although claim 3 has been amended for other purposes, Applicants also disagree with the rejection of the previous wording of claim 3 on page 3 of the Office Action because this claim was entirely clear as previously worded. To illustrate, Applicants refer to the exemplary embodiment of Figure 13 and paragraph 0089 of the Specification which describes how in this embodiment "reconfigurable communications infrastructure 1300 includes at least four *separate signal processing circuits* (*e.g.,* four separate circuit cards) 1310, 1312, 1314 and 1316 **[and]** signal processing circuit 1310 includes a single ASIC device in the form of *a FPGA 1320*, signal processing circuit 1312 includes a single processor device (*e.g.*, CPU, microprocessor), signal processing circuit 1314 includes an array of four ASIC devices in the form of *four FPGAs 1320*, and signal processing circuit 1316 includes an array of two ASIC devices in the form of *two FPGAs 1320*" (emphasis added). Accordingly, referring to the non-limiting example of Figure 13, the previous wording of claim 3 recited (in part) "providing said two or more FPGA devices **[*e.g.*, 1320]** by providing two or more signal processing circuits **[*e.g.*, 1310, 1314 or 1316]** each one of said two or more signal processing circuits **[*e.g.*, 1310, 1314 or 1316]** comprising at least one FPGA device **[*e.g.*, 1320]**." In other words, two or more FPGA devices are provided by supplying two or more signal processing circuits (*e.g.,* as two separate circuit cards) that each itself includes at least one FPGA device. The previous wording of claim 3 was thus not only clear, but also consistent with the description and illustrated embodiments of the Specification.

Next, the interpretation of claim 4 made on pages 3-4 of the Office Action is incorrect, and the present language of this claim is clear and definite for the following reasons. To illustrate, Applicants refer to the exemplary embodiment of Figure 15 and paragraph 0095 of the Specification that describes how in this embodiment "*reconfigurable signal processing circuit* 1314 includes four FPGA devices that may be configured to communicate with each other in a manner as described for FPGA devices 102, 104, 106 and 108 of Figures 1-12 herein, *i.e.,* with

duplex serial data communication links 1520 provided between each given two of FPGA devices 102, 104, 106 and 108 (*e.g.,* via high speed serial I/O connections in the form of MGTs), and with each FPGA being provided with *a packet router* interface switch matrix ("PRISM") to route packets between each of the individual FPGA devices via respective *duplex serial data communication links 1520* as shown" (emphasis added). Accordingly, referring to the non-limiting example of Figure 15, amended dependent claim 4 recites (in part) "said packet router of each one of said two or more FPGA devices **[*e.g.,* 1320]** of each given one of said signal processing circuits **[*e.g.,* 1314]** being coupled **[*e.g.,* via data communication links 1520]** to each respective packet router of each of the other of said two or more FPGA devices **[*e.g.,* 1320]** of said same given one of said signal processing circuits **[*e.g.,* 1314]**; and wherein said method further comprises using said packet router of each given one of said two or more FPGA devices **[*e.g.,* 1320]** of each given one of said signal processing circuits **[*e.g.,* 1320]** to communicate data packets **[*e.g.,* across data communication links 1520]** within said given signal processing circuit by routing data packets to and from each other of said two or more FPGA devices **[*e.g.,* 1320]** of the same given one of said signal processing circuits **[*e.g.,* 1314]**". In other words, the packet router of each of the FPGA devices of a given signal processing circuit is coupled to the packet router of each of the other FPGA devices of the same given signal processing circuit, for example, by the communication links 1520 of Figure 15. Claim 4 is thus not only clear, but also consistent with the description and illustrated embodiments of the Specification. Similar reasoning applies the 35 USC Section 112 rejection of claims 5, 19 and 20.

With regard to claim 15, this claim has been amended to recite (in part) "performing said third computing task with said third computing cluster.

As shown above, all of the pending claims are clear and definite. Favorable reconsideration is requested.

C. The 35 USC Section 103 Rejections

Amended independent claim 1 recites:

> A method, comprising: providing two or more separate signal processing circuits, each one of said two or more signal processing circuits including multiple ASIC devices that each includes a respective packet router; providing a high bandwidth interconnection medium coupled between said signal processing circuits to form a reconfigurable communications infrastructure of said two or more signal processing circuits, the two or more signal processing circuits being *selectively segregatable* from each other, and *the respective ASIC devices* of each one of said two or more signal processing circuits *being directly coupled to* said high bandwidth interconnection medium by *a respective common interface* provided for the ASIC devices of each of said two or more signal processing circuits *with no other processing device intervening between the high bandwidth interconnection medium and said respective ASIC devices*; and selectively communicating data between said two or more signal processing circuits by selectively routing data through the packet router of each of the respective ASIC devices of each one of said signal processing circuits across a first common interface to the high bandwidth interconnection medium and to an other one of said signal processing circuits through a second common interface to the packet router of each of the respective ASIC devices of said other one of said signal processing circuits *without routing said data through any other intervening processing device between each respective ASIC device and the high bandwidth interconnection medium.*

The Office Action cites Col. 5, lines 61-64 of Mukherjee to reject original claim 1. However Mukherjee's "system **10**" is implemented using "SPM methodology **14** [which] is the *software* methodology and tool that implements application designs onto the hybrid network **12**" that is further illustrated in Figure 2 (*see* Col. 5, line 66 to Col. 6, line 1; *see also* Figure 1)(emphasis added). In particular, the Office Action points to the "example network (12) topologies mentioned by Mukherjee" and states that "communications between Mukherjee's network nodes can be said to provide a 'high bandwidth interconnection medium' forming a 'reconfigurable communications infrastructure" (*see* pages 4-5 of the Office Action).

However, unlike amended claim 1, Mukherjee teaches or suggest nothing regarding two or more separate signal processing circuits that each includes multiple ASIC devices that are each *directly coupled to* a high bandwidth interconnection medium by a respective common interface *with no other processing device intervening between the high bandwidth interconnection medium and the respective ASIC devices.* Rather each of the nodes of Mukherjee's network 12 requires an intervening "host machine 22" which connects the node to the network 12 (*see* Figure 2) and which further requires that "one of the nodes 22 functions as a master server 20 in that it provides the interconnection point between the network 12 and the SPM tool 14. It is the master server 20 on which the SPM tool 14 is installed" (*see* Col. 6, lines 24-27).

Thus Mukherjee actually *teaches away* from the recitation of amended claim 1, which relates to a method in which *the respective ASIC devices* of each one of the two or more signal processing circuits *are directly coupled to* the high bandwidth interconnection medium *with no other processing device intervening between the high bandwidth interconnection medium and the respective ASIC devices,* as well as the step of selectively communicating data *between the two or more signal processing circuits* by selectively routing data through the packet router of each of the respective ASIC devices of each one of the signal processing circuits to the packet router of each of the respective ASIC devices of the other one of the signal processing circuits *without routing the data through any other intervening processing device between each respective ASIC device and the high bandwidth interconnection medium* (*see* MPEP 2141.02).

For at least the above reasons, amended independent claim 1, and the claims dependent therefrom are thus not obvious over the cited reference. Similar reasoning applies to amended independent claims 16, 27 and 31, as well as the claims dependent from these amended independent claims.

The Office Action admits that a number of the claimed limitations are missing from Mukherjee, but nonetheless relies on "Official Notice" to satisfy these deficiencies of the reference and reject numerous claims. In particular the Office Action cites to "Official Notice" on four separate occasions (*see* the Office Action at pages 5, 6 and 7). Applicants note that MPEP 2144.03 states that "[o]fficial notice unsupported by documentary evidence should only be taken by the examiner where the facts asserted to be well-known, or to be common knowledge in the art are capable of **instant and unquestionable demonstration** as being well-known [and] the notice of facts beyond the record which may be taken by the examiner must be "capable of such instant and unquestionable demonstration as to defy dispute" (emphasis added). Thus, "[i]t would not be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known" (*see Id.*) (emphasis added). Importantly, "[t]he Board cannot simply reach conclusions based on its own understanding or experience-or on its assessment of what would be basic knowledge or common sense" (*see Id.*) **Rather, "[i]f the examiner is relying on personal knowledge to support the finding of what is known in the art, the examiner must provide an affidavit or declaration setting forth**

specific factual statements and explanation to support the finding" (*see Id.*). Thus, if rejections based on "Official Notice" are to be maintained in the next Office Action, the Examiner is respectfully requested to either provide one or more references in support of the rejections, or an affidavit averring facts within the personal knowledge of the Examiner.

Favorable reconsideration is requested.

D. The Dependent Claims

The dependent claims include additional limitations that render these claims even further nonobvious over Mukherjee. For example, amended dependent claim 3 recites "wherein said two or more signal processing circuits are physically segregated from each other by at least one of being positioned *in different rooms of a given building or facility from each other, or being positioned in different compartments of a given mobile vehicle from each other*" (emphasis added). Similar reasoning applies to amended dependent claims 18, 30 and 34.

As another example, amended dependent claim 13 recites, in part, "configuring said first and second *signal processing circuits* to perform a first computing task together as *a first computing cluster*", "providing at least two additional separate signal processing circuits as a third signal processing circuit including multiple FPGA devices and a fourth signal processing circuit including multiple FPGA devices, *the first, second, third and fourth signal processing circuits being selectively segregatable from each other*", and "dynamically configuring said third and fourth separate *signal processing circuits* in real time to perform a second computing task together as *a second computing cluster*, said second computing task being different than said first computing task; and *simultaneously performing* said first computing task with said first computing cluster and said second computing task with said second computing cluster" (emphasis added). Similar reasoning applies to amended dependent claims 14-15 which depend amended dependent claim 13, and which include additional "reconfiguring" limitations.

E. Conclusion

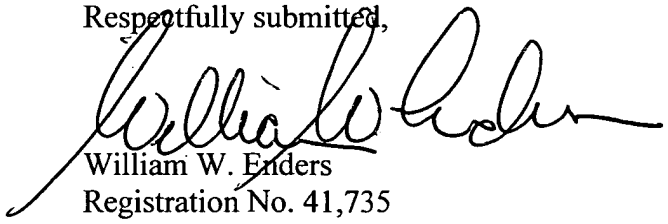
The pending claims have been shown above to be allowable over the cited references. Applicants therefore respectfully submit that claims are in condition for allowance. Reconsideration of the application and claims is courteously solicited.

Please find attached a check in the amount of $130.00 for the Request For Extension Of Time. No additional fees are believed to be due with respect to the enclosed materials. However, should any fees under 37 CFR 1.16-1.21 be required for any reason relating to the enclosed materials, the Commissioner is authorized to deduct such fees from Deposit Account No. 10-1205/LCOM:057.

In accordance with 37 CFR 1.136(a)(3), the Commissioner is authorized to treat any concurrent or future reply that requires a petition for an extension of time under 37 CFR 1.126(a) to be timely, as incorporating a petition for extension of time for the appropriate length of time, and the Commissioner is authorized to deduct any requisite extension of time fees under 37 CFR 1.16 to 1.21 from Deposit Account No. 10-1205/ LCOM:057.

The examiner is invited to contact the undersigned at the phone number indicated below with any questions or comments, or to otherwise facilitate expeditious and compact prosecution of the application.

Respectfully submitted,



William W. Enders
Registration No. 41,735
Attorney for Applicant

O'KEEFE, EGAN, PETERMAN & ENDERS
1101 Capital of Texas Highway South
Building C, Suite 200
Austin, Texas 78746
(512) 347-1611
FAX: (512) 347-1615

Ex. A

Definition of: **ASIC**

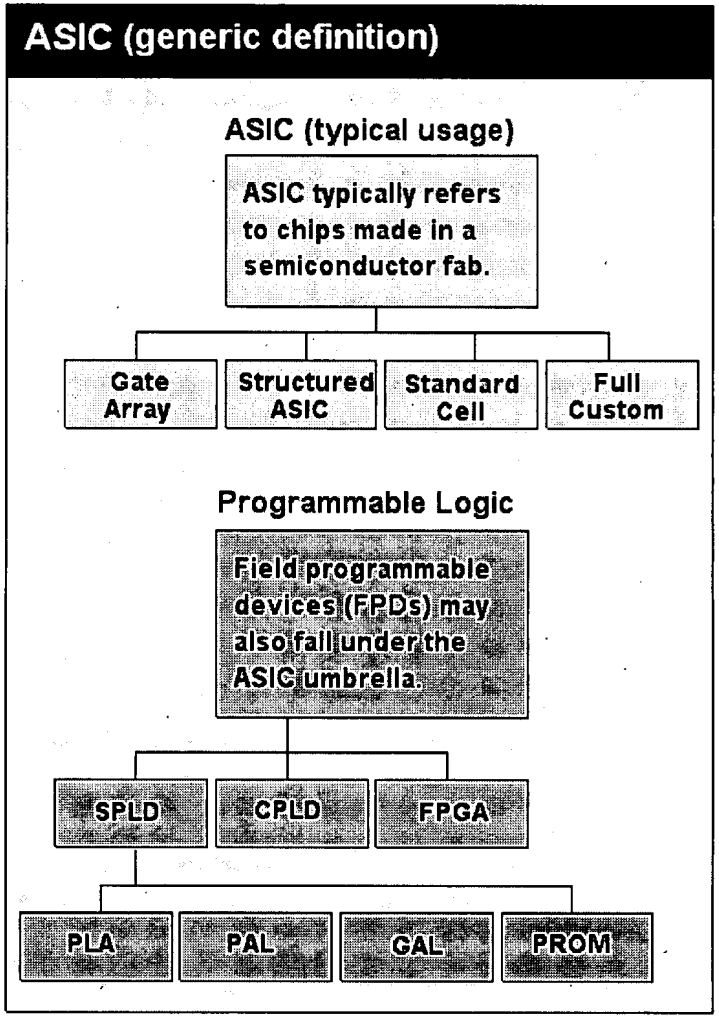
(**A**pplication **S**pecific **I**ntegrated **C**ircuit) Pronounced "**a**-sick." A chip that is custom designed for a specific application rather than a general-purpose chip such as a microprocessor. The use of ASICs improve performance over general-purpose CPUs, because ASICs are "hardwired" to do a specific job and do not incur the overhead of fetching and interpreting stored instructions. However, a standard cell ASIC may include one or more microprocessor cores and embedded software, in which case, it may be referred to as a "system on a chip" (SoC).

A full custom ASIC chip is the most costly, and like standard cell ASICs, use a custom-designed mask for every layer in the chip. Unlike standard cells, designers of a full custom device have total control over the size of every transistor forming every logic gate, so they can "fine tune" each gate for optimum performance. Thus, a full custom ASIC performs electronic operations as fast as it is possible to do so, providing that the circuit design is efficiently architected.

Several Alternatives

Today, full custom ASICs represent a small percentage of the ASIC market because gate arrays, structured ASICs and standard cells turn circuit designs into working chips much faster and at much less cost. Such chips have greatly improved in speed over the years and provide the necessary performance for many applications. The speed advantage of a full custom ASIC is not as relevant as it was in the past. It is used primarily for devices such as microprocessors that must run as fast as possible and will be produced in huge quantities.

Also promoting the decline of full custom ASICs are chip manufacturers that make generic chips containing all the necessary functions for specific mass market products such as DVDs, CDs, digital cameras, etc. See structured ASIC, gate array, standard cell, ASSP, PLD, adaptive computing and CSIC.



Types of ASICs

ASICs can be defined as made in a semiconductor fab only or they can embrace the programmable logic market as well. *(Diagram courtesy of Clive Maxfield, www.techbites.com)*

RELATED TERMS:

adaptive computing
ASSP
CSIC
gate array
PLD
standard cell
structured ASIC

Search: Search Encyclopedia Browse the index

ABOUT PCMAG.COM

Contact Us
About Us
Newsletters
RSS Feeds
Advertise
Reprints & Permissions
Site Map

PC MAGAZINE DIGITAL EDITION

Issue Index
Customer Service
Subscribe

SUBSCRIBE
Get PCMag for only $1 an issue!

REVIEWS

Editors' Choice
Desktops
Laptops
Cell Phones
Printers
Networking
Software
Digital Cameras
HDTV
Netbooks
Security
MP3 Players
Windows 7
Shop for Tech
Review Roundups
Inside PC Labs

DOWNLOADS

Shareware
Utilities

NEWS & OPINION

Tech News
Lance Ulanoff
John C. Dvorak
Dan Costa
Sascha Segan
Tim Bajarin
Michael J. Miller

PCMAG NETWORK

AppScout
ExtremeTech
Gearlog
GoodCleanTech
PCMag.com
Security Watch
Smart Device Central
TechSaver
PCMag Radio & After Hours
CrankyGeeks
DL.TV
PCMag Mobile

TIPS

Ask the Experts
Build It/DIY
Buying Guide
Encyclopedia
Forum

PCMAG EVERYWHERE

Twitter (@pcmag)
TweetMixx
Facebook
YouTube
Mixx
Google Buzz

BUSINESS

Whitepapers

Contact Us
Ziff Davis, Inc.
Link to Us

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JERRY W. YANCEY ET AL.
Filed:	NOVEMBER 16, 2006
For:	RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS
Serial No.:	11/600,934
Group Art Unit:	2112
Examiner:	BAKER, STEPHEN M.
Atty Dkt:	LCOM:057

Pursuant to 37 C.F.R. 1.8, I certify that this correspondence is being deposited with the U.S. Postal Service in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313 on the date below:

10/25/10 Mark Spivak

Date Name

REQUEST FOR EXTENSION OF TIME TO RESPOND TO OFFICE ACTION DATED JUNE 23, 2010

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

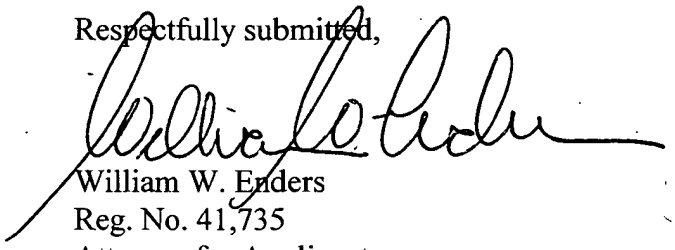
Pursuant to 37 C.F.R. §1.136(a), Applicants petition for an extension of time for one month(s) to and including October 25, 2010, in which to respond to the Office Action dated June 23, 2010.

Please find attached a check in the amount of $130.00. Should any additional fees under 37 C.F.R. §1.16 to 1.21 be required for any reason relating to the enclosed materials, or should an overpayment be included herein, the Commissioner is authorized to deduct or credit said

11/01/2010 SDENBOB3 00000018 11600934
01 FC:1251 130.00 OP

fees from or to Deposit Account No. 10-1205/LCOM:057.

Respectfully submitted,



William W. Enders
Reg. No. 41,735
Attorney for Applicants

O'KEEFE, EGAN, PETERMAN & ENDERS, LLP
1101 South Capital of Texas Highway
Building C, Suite 200
Austin, Texas 78746
512/347-1611
FAX: 512/347-1615

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
11/600,934	11/16/2006	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☒ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	300

APPLICATION AS AMENDED – PART II

AMENDMENT 11/01/2010	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 34	Minus	** 34	= 0	X $ =		OR	X $52=	0
Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X $ =		OR	X $220=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

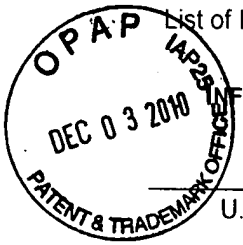
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/TAMMY MCBETH BROWN/



Form PTO-1449 (modified)	Atty. Docket No. LCOM:057	Serial No. 11/600,934
List of Patents and Publications for Applicant's **INFORMATION DISCLOSURE STATEMENT** (Use several sheets if necessary)	Applicant JERRY YANCEY ET AL.	
	Filing Date: 11/16/06	Group: 2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Pages 1-3*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A58	7,518,396	4/14/09	Kondapalli et al.			6/25/07

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C25	Yancey et al, "Systems And Methods For Data Transfer", Serial No. 11/529,713, Filed September 28, 2006, Preliminary Amendment; December 22, 2006, 11 pgs.
	C26	Yancey et al, "Systems And Methods For Data Transfer", Serial No. 11/529,713, Filed September 28, 2006, Office Action, February 19, 2009, 12 pgs.
	C27	Yancey et al, "Systems And Methods For Data Transfer", Serial No. 11/529,713, Filed September 28, 2006, Amendment; Response To Office Action, May 19, 2009, 17 pgs.
	C28	Yancey et al, "Systems And Methods For Data Transfer", Serial No. 11/529,713, Filed September 28, 2006, Office Action, August 19, 2009, 5 pgs.
	C29	Yancey et al, "Systems And Methods For Data Transfer", Serial No. 11/529,713, Filed September 28, 2006, Response To Office Action, August 25, 2009, 4 pgs.
	C30	Yancey et al, "Systems And Methods For Data Transfer", Serial No. 11/529,713, Filed September 28, 2006, Office Action, October 2, 2009, 3 pgs.
	C31	Yancey et al, "Systems And Methods For Data Transfer", Serial No. 11/529,713, Filed September 28, 2006, Response To Advisory Action, October 14, 2009, 4 pgs.
	C32	Yancey et al, "Systems And Methods For Data Transfer", Serial No. 11/529,713, Filed September 28, 2006, Notice of Allowance And Fees Due, December 4, 2009, 4 pgs.
	C33	Yancey et al, "Systems And Methods For Interconnection Of Multiple FPGA Devices", Serial No. 10/843,226, Filed May 11, 2004, Preliminary Amendment, November 14, 2006, 19 pgs.

Examiner:	**Date Considered:**

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449 (modified)	Atty. Docket No. LCOM:057	Serial No. 11/600,934
List of Patents and Publications for Applicant's **INFORMATION DISCLOSURE STATEMENT** (Use several sheets if necessary)	Applicant JERRY YANCEY ET AL.	
	Filing Date: 11/16/06	Group: 2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Pages 1-3*

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C34	Yancey et al, "Systems And Methods For Interconnection Of Multiple FPGA Devices", Serial No. 10/843,226, Filed May 11, 2004, Second Preliminary Amendment, November 29, 2006, 3 pgs.
	C35	Yancey et al, "Systems And Methods For Interconnection Of Multiple FPGA Devices", Serial No. 10/843,226, Filed May 11, 2004, Office Action, January 4, 2007, 25 pgs.
	C36	Yancey et al, "Systems And Methods For Interconnection Of Multiple FPGA Devices", Serial No. 10/843,226, Filed May 11, 2004, Amendment and response To Office Action, May 4, 2007, 32 pgs.
	C37	Yancey et al, "Systems And Methods For Interconnection Of Multiple FPGA Devices", Serial No. 10/843,226, Filed May 11, 2004, Office Action, July 27, 2007, 29 pgs.
	C38	Yancey et al, "Systems And Methods For Interconnection Of Multiple FPGA Devices", Serial No. 10/843,226, Filed May 11, 2004, Amendment and Response To Office Action, Septemer 27, 2007, 37 pgs.
	C39	Yancey et al, "Systems And Methods For Interconnection Of Multiple FPGA Devices", Serial No. 10/843,226, Filed May 11, 2004, Office Action, November 6, 2007, 26 pgs.
	C40	Yancey et al, "Systems And Methods For Interconnection Of Multiple FPGA Devices", Serial No. 10/843,226, Filed May 11, 2004, Amendment and Response to Office Action, April 16, 2008, 46 pgs.
	C41	Yancey et al, "Systems And Methods For Interconnection Of Multiple FPGA Devices", Serial No. 10/843,226, Filed May 11, 2004, Notice of Allowance and Fees Due, July 23, 2008, 11 pgs.
	C42	Yancey et al, "Systems And Methods For Writing Data With A Fifo Interface", Serial No. 11/529,712, Filed September 28, 2006, Preliminary Amendment, December 7, 2006, 13 pgs.
	C43	Yancey et al, "Systems And Methods For Writing Data With A Fifo Interface", Serial No. 11/529,712, Filed September 28, 2006, Office Action, April 27, 2007, 17 pgs.
	C45	Yancey et al, "Systems And Methods For Writing Data With A Fifo Interface", Serial No. 11/529,712, Filed September 28, 2006, Amendment and Response To Office Action, July 25, 2007, 19 pgs.
	C46	Yancey et al, "Systems And Methods For Writing Data With A Fifo Interface", Serial No. 11/529,712, Filed September 28, 2006, Office Action, October 22, 2007, 17 pgs.

Examiner:	**Date Considered:**

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449 (modified)	Atty. Docket No. LCOM:057	Serial No. 11/600,934
List of Patents and Publications for Applicant's **INFORMATION DISCLOSURE STATEMENT** (Use several sheets if necessary)	Applicant JERRY YANCEY ET AL.	
	Filing Date: 11/16/06	Group: 2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Pages 1-3*

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C47	Yancey et al, "Systems And Methods For Writing Data With A Fifo Interface", Serial No. 11/529,712, Filed September 28, 2006, RCE and Amendment, March 19, 2008, 26 pgs.
	C48	Yancey et al, "Systems And Methods For Writing Data With A Fifo Interface", Serial No. 11/529,712, Filed September 28, 2006, Notice of Allowance and Fees Due, May 30, 2008, 7 pgs.

Examiner:	**Date Considered:**

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JERRY W. YANCEY ET AL.
Filed:	NOVEMBER 16, 2006
For:	RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS
Serial No.:	11/600,934
Group Art Unit:	2133
Examiner:	UNKNOWN
Atty Dkt:	LCOM:057

Pursuant to 37 C.F.R. 1.8, I certify that this correspondence is being deposited with the U.S. Postal Service in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313

Date 11/15/10 Name Patty Johns

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the document(s) listed on attached Form PTO-1449 be considered by the Examiner and made of record.

In accordance with 37 C.F.R §§ 1.97(g),(h), this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made, and is not to be construed to be an admission that (a) the information cited is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b); and/or (b) that the information cited is, or is considered to be prior art.

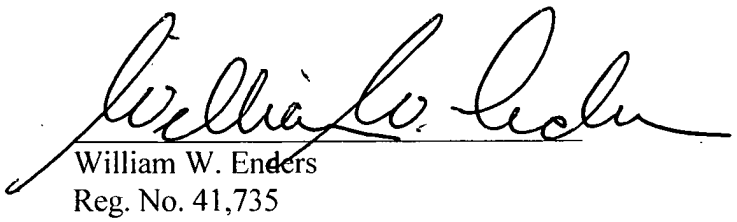
PROSECUTION DOCUMENTS FROM RELATED CASES

Attached hereto as reference C32 to C39 are amendment and office action documents from United States Patent Application Serial No. 10/843,226 (now U.S. Patent No. 7,444,454) from which the present application claims priority. Also attached as references C25 to C31, and C40 to C44, are references from United States Patent Application Serial No. 11/529,712 (now U.S. Patent No. 7,426,599) and United States Patent Application Serial No. 11/529,713 (now U.S. Patent No. 7,689,757) respectively, which are each continuation applications claiming priority to U.S. Patent Application Serial No. 10/843,226. These application serial numbers 11/529,712 and 11/529,713 were previously cited as references C21 and C22 in the present application.

Pursuant to §1.97(c), this Information Disclosure Statement is being submitted after the period specified in §1.97(b), but prior to the mailing of the final action under §1.113, a notice of allowance under §1.311, or an action that otherwise closes prosecution of the application, and pursuant to 37 C.F.R. §1.97(c)(2), the fee set forth in §1.17(p) ($180) is enclosed, however, should any additional fees under 37 C.F.R. §§ 1.16 to 1.21 be deemed necessary for any reason relating to these materials, the Commissioner is hereby authorized to deduct said fees from Deposit Account No. 10-1205/LCOM:057.

Applicant respectfully requests that the listed document(s) be made of record in the present case.

Respectfully submitted,



William W. Enders
Reg. No. 41,735
Attorney for Applicant

O'KEEFE, EGAN, PETERMAN & ENDERS, LLP
1101 Capital of Texas Highway South
Building C, Suite 200
Austin, Texas 78746
(512) 347-1611
FAX: (512) 347-1615

Enclosures

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

36275 7590 01/24/2011

O'KEEFE, EGAN, PETERMAN & ENDERS LLP
1101 CAPITAL OF TEXAS HIGHWAY SOUTH
#C200
AUSTIN, TX 78746

EXAMINER	
BAKER, STEPHEN M	
ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 01/24/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/600,934	11/16/2006	Jerry W. Yancey	LCOM:057	4821

TITLE OF INVENTION: RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	04/25/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

36275 7590 01/24/2011

O'KEEFE, EGAN, PETERMAN & ENDERS LLP
1101 CAPITAL OF TEXAS HIGHWAY SOUTH
#C200
AUSTIN, TX 78746

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/600,934	11/16/2006	Jerry W. Yancey	LCOM:057	4821

TITLE OF INVENTION: RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	04/25/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
BAKER, STEPHEN M	2112	714-776000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/600,934	11/16/2006	Jerry W. Yancey	LCOM:057	4821

36275 7590 01/24/2011

O'KEEFE, EGAN, PETERMAN & ENDERS LLP
1101 CAPITAL OF TEXAS HIGHWAY SOUTH
#C200
AUSTIN, TX 78746

EXAMINER	
BAKER, STEPHEN M	
ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 01/24/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 818 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 818 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No. 11/600,934	Applicant(s) YANCEY ET AL.	
	Examiner Stephen M. Baker	Art Unit 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed 01 November 2010*.

2. ☒ The allowed claim(s) is/are *1-34*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 120310
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Stephen M. Baker/
Primary Examiner
Art Unit: 2112

Form PTO-1449 (modified)	Atty. Docket No. LCOM:057	Serial No. 11/600,934
List of Patents and Publications for Applicant's INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	Applicant JERRY YANCEY ET AL.	
	Filing Date: 11/16/06	Group: 2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Pages 1-3*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date if App.
	A58	7,518,396	4/14/09	Kondapalli et al.			6/25/07

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C25	Yancey et al, "Systems And Methods For Data Transfer", Serial No. 11/529,713, Filed September 28, 2006, Preliminary Amendment; December 22, 2006, 11 pgs.
	C26	Yancey et al, "Systems And Methods For Data Transfer", Serial No. 11/529,713, Filed September 28, 2006, Office Action, February 19, 2009, 12 pgs.
	C27	Yancey et al, "Systems And Methods For Data Transfer", Serial No. 11/529,713, Filed September 28, 2006, Amendment; Response To Office Action, May 19, 2009, 17 pgs.
	C28	Yancey et al, "Systems And Methods For Data Transfer", Serial No. 11/529,713, Filed September 28, 2006, Office Action, August 19, 2009, 5 pgs.
	C29	Yancey et al, "Systems And Methods For Data Transfer", Serial No. 11/529,713, Filed September 28, 2006, Response To Office Action, August 25, 2009, 4 pgs.
	C30	Yancey et al, "Systems And Methods For Data Transfer", Serial No. 11/529,713, Filed September 28, 2006, Office Action, October 2, 2009, 3 pgs.
	C31	Yancey et al, "Systems And Methods For Data Transfer", Serial No. 11/529,713, Filed September 28, 2006, Response To Advisory Action, October 14, 2009, 4 pgs.
	C32	Yancey et al, "Systems And Methods For Data Transfer", Serial No. 11/529,713, Filed September 28, 2006, Notice of Allowance And Fees Due, December 4, 2009, 4 pgs.
	C33	Yancey et al, "Systems And Methods For Interconnection Of Multiple FPGA Devices", Serial No. 10/843,226, Filed May 11, 2004, Preliminary Amendment, November 14, 2006, 19 pgs.

Examiner: /Stephen Baker/	Date Considered: 01/20/2011

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

Form PTO-1449 (modified)	Atty. Docket No. LCOM:057	Serial No. 11/600,934
List of Patents and Publications for Applicant's **INFORMATION DISCLOSURE STATEMENT** (Use several sheets if necessary)	Applicant JERRY YANCEY ET AL.	
	Filing Date: 11/16/06	Group: 2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Pages 1-3*

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C34	Yancey et al, "Systems And Methods For Interconnection Of Multiple FPGA Devices", Serial No. 10/843,226, Filed May 11, 2004, Second Preliminary Amendment, November 29, 2006, 3 pgs.
	C35	Yancey et al, "Systems And Methods For Interconnection Of Multiple FPGA Devices", Serial No. 10/843,226, Filed May 11, 2004, Office Action, January 4, 2007, 25 pgs.
	C36	Yancey et al, "Systems And Methods For Interconnection Of Multiple FPGA Devices", Serial No. 10/843,226, Filed May 11, 2004, Amendment and response To Office Action, May 4, 2007, 32 pgs.
	C37	Yancey et al, "Systems And Methods For Interconnection Of Multiple FPGA Devices", Serial No. 10/843,226, Filed May 11, 2004, Office Action, July 27, 2007, 29 pgs.
	C38	Yancey et al, "Systems And Methods For Interconnection Of Multiple FPGA Devices", Serial No. 10/843,226, Filed May 11, 2004, Amendment and Response To Office Action, Septemer 27, 2007, 37 pgs.
	C39	Yancey et al, "Systems And Methods For Interconnection Of Multiple FPGA Devices", Serial No. 10/843,226, Filed May 11, 2004, Office Action, November 6, 2007, 26 pgs.
	C40	Yancey et al, "Systems And Methods For Interconnection Of Multiple FPGA Devices", Serial No. 10/843,226, Filed May 11, 2004, Amendment and Response to Office Action, April 16, 2008, 46 pgs.
	C41	Yancey et al, "Systems And Methods For Interconnection Of Multiple FPGA Devices", Serial No. 10/843,226, Filed May 11, 2004, Notice of Allowance and Fees Due, July 23, 2008, 11 pgs.
	C42	Yancey et al, "Systems And Methods For Writing Data With A Fifo Interface", Serial No. 11/529,712, Filed September 28, 2006, Preliminary Amendment, December 7, 2006, 13 pgs.
	C43	Yancey et al, "Systems And Methods For Writing Data With A Fifo Interface", Serial No. 11/529,712, Filed September 28, 2006, Office Action, April 27, 2007, 17 pgs.
	C45	Yancey et al, "Systems And Methods For Writing Data With A Fifo Interface", Serial No. 11/529,712, Filed September 28, 2006, Amendment and Response To Office Action, July 25, 2007, 19 pgs.
	C46	Yancey et al, "Systems And Methods For Writing Data With A Fifo Interface", Serial No. 11/529,712, Filed September 28, 2006, Office Action, October 22, 2007, 17 pgs.

Examiner: /Stephen Baker/	**Date Considered:** 01/20/2011

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

Form PTO-1449 (modified)	Atty. Docket No. LCOM:057	Serial No. 11/600,934
List of Patents and Publications for Applicant's **INFORMATION DISCLOSURE STATEMENT** (Use several sheets if necessary)	Applicant JERRY YANCEY ET AL.	
	Filing Date: 11/16/06	Group: 2133

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page*	*See Pages 1-3*

Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C47	Yancey et al, "Systems And Methods For Writing Data With A Fifo Interface", Serial No. 11/529,712, Filed September 28, 2006, RCE and Amendment, March 19, 2008, 26 pgs.
	C48	Yancey et al, "Systems And Methods For Writing Data With A Fifo Interface", Serial No. 11/529,712, Filed September 28, 2006, Notice of Allowance and Fees Due, May 30, 2008, 7 pgs.

Examiner: /Stephen Baker/	**Date Considered:** 01/20/2011

EXAMINER: initial if reference considered, whether or not citation is in conformance with MPEP609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.B./

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11600934	YANCEY ET AL.
	Examiner	**Art Unit**
	Stephen M Baker	2112

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	06/18/2010	01/20/2011							
1	1	✓	=							
2	2	✓	=							
3	3	✓	=							
11	4	✓	=							
12	5	✓	=							
4	6	✓	=							
5	7	✓	=							
6	8	✓	=							
7	9	✓	=							
8	10	✓	=							
9	11	✓	=							
10	12	✓	=							
13	13	✓	=							
14	14	✓	=							
15	15	✓	=							
16	16	✓	=							
17	17	✓	=							
26	18	✓	=							
23	19	✓	=							
24	20	✓	=							
18	21	✓	=							
19	22	✓	=							
20	23	✓	=							
25	24	✓	=							
21	25	✓	=							
22	26	✓	=							
27	27	✓	=							
28	28	✓	=							
29	29	✓	=							
30	30	✓	=							
31	31	✓	=							
33	32	✓	=							
34	33	✓	=							
32	34	✓	=							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	11600934	YANCEY ET AL.
	Examiner	**Art Unit**
	Stephen M Baker	2112

SEARCHED			
Class	**Subclass**	**Date**	**Examiner**
714	4, 5	06/19/2010	SMB
714	4, 5	01/20/2011	SMB

SEARCH NOTES		
Search Notes	**Date**	**Examiner**

INTERFERENCE SEARCH			
Class	**Subclass**	**Date**	**Examiner**
714	4	01/20/2011	SMB

Issue Classification

Application/Control No.	Applicant(s)/Patent Under Reexamination
11600934	YANCEY ET AL.
Examiner	**Art Unit**
Stephen M Baker	2112

ORIGINAL		INTERNATIONAL CLASSIFICATION														
CLASS	SUBCLASS	CLAIMED									NON-CLAIMED					
714	4	G	0	6	F	13 / 00 (2006.01.01)										

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				

☐ Claims renumbered in the same order as presented by applicant ☒ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	17	34	33										
2	2	26	18	32	34										
3	3	23	19												
11	4	24	20												
12	5	18	21												
4	6	19	22												
5	7	20	23												
6	8	25	24												
7	9	21	25												
8	10	22	26												
9	11	27	27												
10	12	28	28												
13	13	29	29												
14	14	30	30												
15	15	31	31												
16	16	33	32												

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 34	
/Stephen M Baker/ Primary Examiner.Art Unit 2112 (Primary Examiner)	01/20/2011 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 2

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

36275 7590 01/24/2011

O'KEEFE, EGAN, PETERMAN & ENDERS LLP
1101 CAPITAL OF TEXAS HIGHWAY SOUTH
#C200
AUSTIN, TX 78746

02/28/2011 EEKUBAY2 00000109 11600934

01 FC:1501 1510.00 OP
02 FC:1504 300.00 OP

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Marty Jones	(Depositor's name)
	(Signature)
2/23/11	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/600,934	11/16/2006	Jerry W. Yancey	LCOM:057	4821

TITLE OF INVENTION: RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	04/25/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
BAKER, STEPHEN M	2112	714-776000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 O'Keefe, Egan, Peterman & Enders LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

L-3 Communications Integrated Systems, L.P. Greenville, Texas

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☒ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 10-1205 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature William W. Enders Date 2/23/2011

Typed or printed name William W. Enders Registration No. 41,735

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Issue Classification

Application/Control No.	Applicant(s)/Patent Under Reexamination
11600934	YANCEY ET AL.
Examiner	**Art Unit**
Stephen M Baker	2112

ORIGINAL		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
714	4	G 0 6 F 13 / 00 (2006.01)	

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				

☐ Claims renumbered in the same order as presented by applicant ☒ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	17	34	33										
2	2	26	18	32	34										
7	3	23	19												
11	4	24	20												
12	5	18	21												
4	6	19	22												
5	7	20	23												
6	8	25	24												
3	9	21	25												
8	10	22	26												
9	11	27	27												
10	12	28	28												
13	13	29	29												
14	14	30	30												
15	15	31	31												
16	16	33	32												

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	34	
/Stephen M Baker/ Primary Examiner.Art Unit 2112	01/20/2011	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/600,934	04/05/2011	7921323	LCOM:057	4821

36275 7590 03/16/2011

O'KEEFE, EGAN, PETERMAN & ENDERS LLP
1101 CAPITAL OF TEXAS HIGHWAY SOUTH
#C200
AUSTIN, TX 78746

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 1104 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Jerry W. Yancey, Rockwall, TX;
Yea Zong Kuo, Rockwall, TX;

PTO/SB/123 (04-15)
Approved for use through 01/31/2018. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

CHANGE OF CORRESPONDENCE ADDRESS
Patent

Address to:
Mail Stop Post Issue
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Patent Number	7,921,323
Issue Date	4/5/2011
Application Number	11/600,934
Filing Date	11/16/2006
First Named Inventor	Jerry W. Yancey
Attorney Docket Number	LCOM:057

Please change the Correspondence Address for the above-identified patent to:

☒ The address associated with Customer Number: **156195**

OR

☐ **Firm *or* Individual Name**

Address

City | **State** | **ZIP**

Country

Telephone | **Email**

This form cannot be used to change the data associated with a Customer Number. To change the data associated with an existing Customer Number use "Request for Customer Number Data Change" (PTO/SB/124).

This form will not affect any "fee address" provided for the above-identified patent. To change a "fee address" use the "Fee Address Indication Form" (PTO/SB/47).

I am the:

☐ Patentee.

☐ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

☒ Attorney or agent of record. Registration Number 41735.

Signature /William W. Enders/

Typed or Printed Name William W. Enders

Date August 6, 2018 | Telephone 512-347-1611

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	33387328
Application Number:	11600934
International Application Number:	
Confirmation Number:	4821
Title of Invention:	RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS
First Named Inventor/Applicant Name:	Jerry W. Yancey
Customer Number:	36275
Filer:	William W. Enders/Marty Jones
Filer Authorized By:	William W. Enders
Attorney Docket Number:	LCOM:057
Receipt Date:	06-AUG-2018
Filing Date:	16-NOV-2006
Time Stamp:	17:11:19
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Change of Address	7921323.pdf	78274 65590a17a1bc9fb38a766a040d8bbf6c037235b4	no	2

Warnings:

Information:	
Total Files Size (in bytes):	78274

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

AO 120 (Rev. 08/10)

TO:	Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:22-cv-305	8/8/2022	Eastern District of Texas

PLAINTIFF	DEFENDANT
LIONRA TECHNOLOGIES LIMITED	CISCO SYSTEMS, INC.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,916,630	3/29/2011	Lionra Technologies Limited
2	8,566,612	10/22/2013	Lionra Technologies Limited
3	7,921,323	4/5/2011	Lionra Technologies Limited
4	7,302,708	11/27/2007	Lionra Technologies Limited
5	7,685,436	3/23/2010	Lionra Technologies Limited

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

Print Save As... Reset

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:22-cv-319	8/19/2022	Eastern District of Texas

PLAINTIFF	DEFENDANT
LIONRA TECHNOLOGIES LIMITED	HEWLETT PACKARD ENTERPRISE COMPANY; ARUBA NETWORKS, LLC

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,916,630	3/29/2011	Lionra Technologies Limited
2	7,921,323	4/5/2011	Lionra Technologies Limited
3			
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

Print Save As... Reset

AO 120 (Rev. 08/10)

TO:	Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:22-cv-00322	8/19/2022	Eastern District of Texas

PLAINTIFF	DEFENDANT
LIONRA TECHNOLOGIES LIMITED	FORTINET, INC.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,302,708	11/27/2007	Lionra Technologies Limited
2	7,685,436	3/23/2010	Lionra Technologies Limited
3	7,921,323	4/5/2011	Lionra Technologies Limited
4	8,566,612	10/22/2013	Lionra Technologies Limited
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

Print Save As... Reset

AO 120 (Rev. 08/10)

TO:	Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:22-cv-00334	8/29/2022	Eastern District of Texas

PLAINTIFF	DEFENDANT
LIONRA TECHNOLOGIES LIMITED	PALO ALTO NETWORKS, INC.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,685,436	3/23/2010	Lionra Technologies Limited
2	8,566,612	10/22/2013	Lionra Technologies Limited
3	7,921,323	4/5/2011	Lionra Technologies Limited
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

Print Save As... Reset